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EVALUATION TESTING OF SOLID ENCAPSULATED MICROCIRCUITS FOR SPACE APPLICATIONS

FINAL TECHNICAL REPORT
CONTRACT NUMBER NAS8-31627
JUNE 1975 - May 1977

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Prepared For
National Aeronautics and Space Administration
George C. Marshall Space Flight Center
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PREFACE

The work described in this report was performed by the Electronic Parts and Subsystems section of the Boeing Aerospace Company Central Laboratories department during the period between June 1975 and May 1977. The work was performed for the National Aeronautics and Space Administration (NASA), George C. Marshall Space Flight Center under Contract Number NAS8-31627. Mr. Leon Hamiter acted as the NASA Contracting Officer's Representative. Significant technical contributions were made by David Porter, Earl Roberts, Mel Char and George Henderson.

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1.0 INTRODUCTION

Epoxy encapsulated microcircuits are widely used in low cost commercial applications but their use has been avoided in space applications because they have been felt to lack the integrity necessary for reliable operation as compared to hermetically sealed microcircuits. Recent improvements in epoxy encapsulants, particularly the introduction of novolac epoxy, have resulted in elimination of many of the failure mechanisms previously found in plastic encapsulated microcircuits.

This study was conducted to investigate three major areas of concern.

- o What design, processing, packaging and application constraints are necessary in the use of epoxy encapsulated microcircuits?
- o What screening tests are useful to identify high integrity devices?
- o What qualification tests should be used to separate high integrity lots of parts from failure-prone lots?

Various thermal, vibration, thermal cycling and reduced barometric pressure stress tests were performed to obtain electrical, environmental and failure data. Analyses of the data were employed to derive information on environmental and operating design limits to determine the capability of encapsulated microcircuits to perform in space applications and environments. Seven different part types (four TTL, two CMOS, one linear) from five different manufacturers were subjected to single, multiple and combinational environmental stress levels to derive answers to the following questions.

- o What failure mechanisms unique to encapsulated microcircuits exist?
- o How believable are suppliers claims of improved reliability?
- o What stress tests and screens can be used to identify potential early failures (e.g. freak population)?
- o What stress tests and screens should be avoided to prevent unwanted life degradation?

2.0 SUMMARY AND CONCLUSIONS

2.1 Program Approach

Novolac encapsulated microcircuits of three different types from 5 different manufacturers were procured and tested using MIL-specification screens and environmental stresses. The parts purchased were:

		Manufacturer	Manufacturer Code
TTL	7400	Texas Instr.	A
	5400	Signetics	B
	5400	National	C
	7400	ITT	D
CMOS	4007	RCA	E
	4007	National	C
Linear	741	RCA	E

5 each were subjected to construction analysis. 495 each (Group 101) were screened to JAN Level B requirements, including temperature cycling, centrifuge, burn-in and electrical measurement (called M1) at -55°C, +25°C, and +125°C. Of the parts which passed the JAN Level B screening, 325 each were subjected to seven different environmental stress test sequences which consisted of MIL-specification environmental tests followed by electrical measurements at -55°C, 25°C, and 125°. The environmental stresses were as shown in Figure 2-1.

Failed parts were subjected to failure analysis to determine the cause of failure.

The intent of this program was to define and identify potential tests and screens that could be used advantageously with epoxy encapsulated microcircuits. It was not the intent of the program to perform a reliability evaluation on the specific device types selected.

2.2 Summary of Results

The single most prominent result derived from this program was the determination that novolac-encapsulated digital bipolar TTL microcircuits are of very high integrity -- so high that relatively few failures occurred for causes traceable to the use of epoxy encapsulants. Generally it was only by raising the stress levels to obviously destructive levels that sizable numbers of failures could be induced. CMOS devices were very unstable and should not be evaluated further. Linear devices showed promise but also showed problems that should be explored further.

Three of the environmental test cells produced no valid failures at all - Groups 203 (Vibration), 204 (Vacuum Operating Life), and 205 (Low Temperature Operating Life). The remainder of the test cells produced the following types of failures.

- o Open ball bond
  - -- peripheral opens
  - -- plastic plague
- o Channeling (CMOS only)
- o Broken wires
- o Thermal Runaway (Linear only)
- o Stress Corrosion Cracking
- o Ruptured Encapsulant

Group 201	o Thermal Shock: 15 cycles from -65°C to +150°C o M2 (Electrical Measurement at -55°C, 25°C, 125°C) o 10 day Moisture Resistance o M3 o 1000 hour Operating Life at +5°C o M4 o 1000 hour Operating Life at +125°C o M5
Group 202	o 1000 Temperature Cycles from -55°C to +125°C o M2 o 1000 Temperature Cycles from -55°C to +125°C o M3 o 1000 Temperature Cycles from -65°C to +150°C o M4 o 1000 Temperature Cycles from -65°C to +200°C o M5
Group 203	o Vibration - 3 axes at 20g o M2 o Vibration - 3 axes at 50g o M3 o Vibration - 3 axes at 70g o M4
Group 204	o 48 hour Operating Life at 1.09 mm Hg (Vacuum) o M2 o 240 hour Operating Life at 1.09 mm Hg o M3 o 48 hour Operating Life at $1x10^{-6}$ mm Hg o M4 o 240 hour Operating Life at $1x10^{-6}$ mm Hg o M5
Group 205	o 240 hour Operating Life at +5°C o M2 o 760 hour Operating Life at +5°C o M3 o 240 hour Operating Life at -55°C o M4 o 760 hour Operating Life at -55°C o M5
Group 206	o 1000 hour Operating Life at 125°C o M2 o 1000 hour Operating Life at 150°C o M3 o 1000 hour Operating Life at 175°C o M4 o 1000 hour Operating Life at 200°C o M5
Group 207	o 1000 Temperature Cycles from -55°C to +125°C o M2 o 48 hour Operating Life at 1.09 mm Hg o M3 o 1000 hour Operating Life at +5°C o M4 o 1000 hour Operating Life at +125°C o M5

Figure 2-1 Environmental Test Program

2.2 Summary of Results (Continued)

- o Absorbed Moisture (CMOS only)
- o Cracked Die
- o Short circuit on die or in diffusion
- o Shorted MOS capacitor (Linear only)
- o Gate Oxide Short circuit

These failures are reported and described in detail in Section 4. The following discussion treats the significance of the failures in terms of the applied stresses.

2.2.1 Open Ball Bond Failures

A total of nine failures occurred on this program during various environments. It was found convenient to convert the time to failure and the causing stress to equivalent hours at 175°C, the temperature of operating life where most of the failures occurred. This is shown in Figure 2-2. The 1.1 ev activation energy was used. These times to failure can be compared to the normally expected median times to failure for the three major types of bond failure: lifted bonds, peripheral opens, and open aluminum away from bond. At 300°C, these times are respectively 3 hours, 300 hours, and 30,000 hours (Ref 1, 2). At 175°C, these medjan times to failure become 1000 hours, 100,000 hours, and 10,000,000 hours (10^3, 10^5, 10^7). These values are plotted in Figure 2-3 along with the equivalent failure times of the bond failures from this program.

Analysis of Figure 2-3 shows that these bond failures can all be interpreted as freak failures, since they all occur in the "freak" part of the curves and occur in extremely small quantities: less than the 5% percent-defective-allowable called out in MIL-M-38510 for post burn-in lot acceptance.

The so-called "plastic plague" failures were found to represent a new failure mode for ball bonds which is unique to encapsulated microcircuits. It is postulated that were it not for the encapsulant holding the bond tightly to die the bond would fail in the normal lifted bond manner. But because the encapsulant holds the bond in place, bond degradation proceeds beyond normal gold-aluminum embrittlement and a large spongy appearing intermetallic formation occurs under the bond as shown in Figure 2-4. The time to failure could be longer for plastic plague than for lifted bonds, as the presentation in Figure 2-3 hints, but until this is verified by further testing, no conclusion can be drawn about relative time to failure.

2.2.2 Channeling

Channeling of the FET transistors was found to be a predominant failure mechanism in CMOS microcircuits subjected to high temperature operating life tests. Figure 2-5 summarizes the failure percentage that occurred during the environmental test cells involving 125°C operating life or higher It can be seen that the incidence of channeling is unacceptably high.

It was determined experimentally that the channeling that occurred was not caused by impurities resident in the epoxy encapsulant but rather by impurities appearing in the CMOS oxide structure. This was found by stripping the encapsulant off of a channeled device and observing that it was still channeling after the encapsulant was removed. However this does not rule out the possibility that the impurities originated in the encapsulant and migrated into the oxide.

Type of Failure	Group	Electrical Measurement	Prior Stress	Thermal Portion	Equivalent Hours @ 175°C
Lifted Bond	201	M3	10 day Moisture Resistance	120 hrs @ 70°C	0.04 hours
Peripheral Open	202	M3	2000 Temp. Cycles -55°C to +125°C	333 hrs @ 125°C	17 hours
Peripheral Open	202	M5	2000 Temp. Cycles	333 hrs @	
			-55 to 125°C	125°C	17
			-65 to 150°C	150°C	77
			-65 to 200°C	200°C	1432
				Total	1525 hours
Plastic Plague	206	M2	1000 hr @ 125°C	1000 hr @ 125°C	50 hours
Plastic Plague	206	M3	1000 hr @		
			125°C		50
			150°C		230
				Total	280 hours
Plastic Plague	206	M4 (4 parts)	1000 hr @		
			125°C		50
			150°C		230
			175°C		1000
				Total	1280 hours

Figure 2-2

Calculation of Equivalent Hours at 175°C for Program Failures Due to Open Bonds

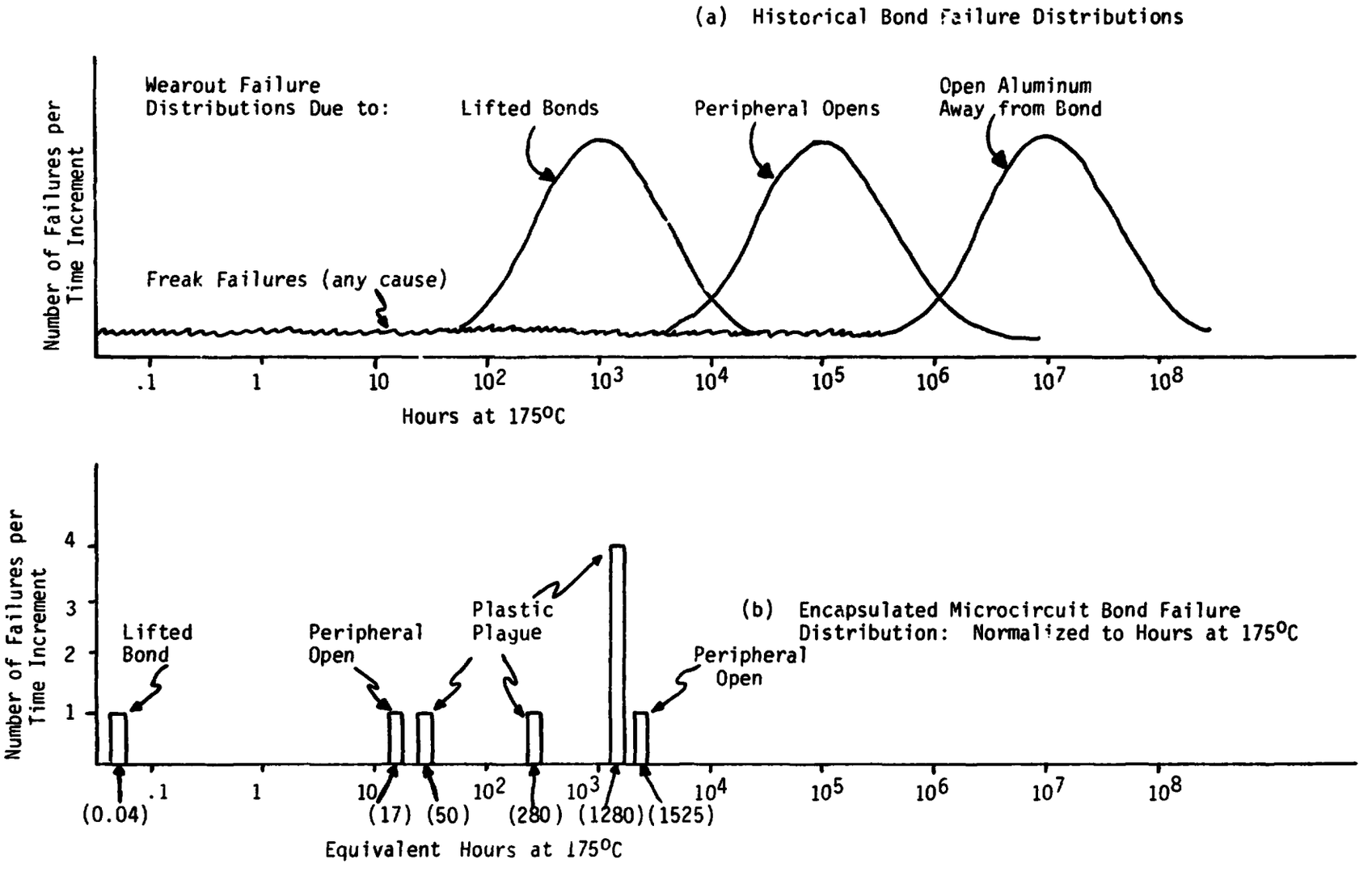

Figure 2-3: Bond Failures Compared to Historical Distributions

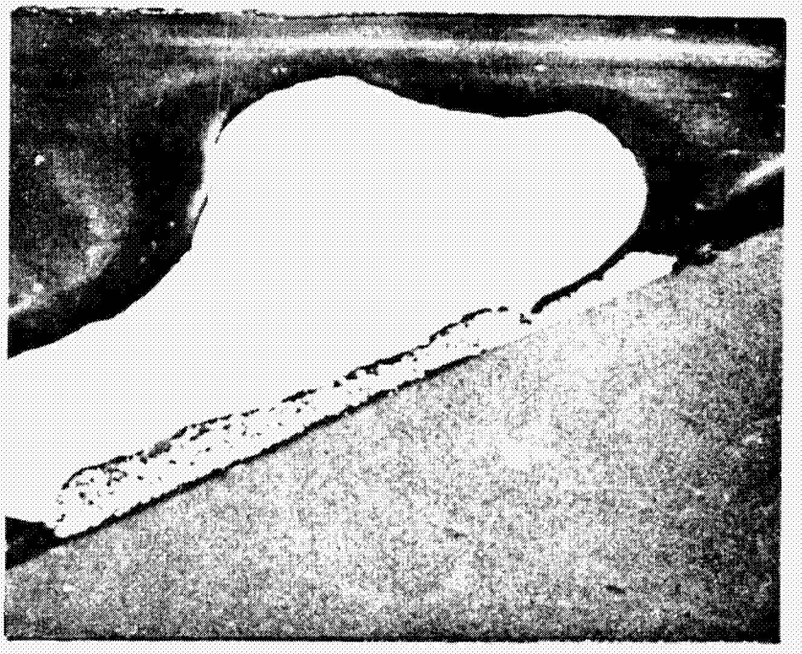

Figure 2-4. Plastic Plague Failure

PERCENT OF EACH TEST CELL THAT FAILED

	1000 hours operating Life at 125°C		1000 hours operating Life at 150°C		1000 hours operating Life at 175°C	
	Manufacturer E	Manufacturer C	Manufacturer E	Manufacturer C	Manufacturer E	Manufacturer C
Group 201	13% (6 out of 47)	49% (24 out of 49)				
Group 206	0 (0 out of 50)	8% (4 out of 50)	0 (0 out of 50)	98% (45 out of 46)	20% (10 out of 50)	
Group 207	4% (2 out of 50)	8% (4 out of 50)				

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Figure 2-5. CMOS Channeling Failures for Various Environmental Stress Cells

2.2.3 Broken Wires

Temperature cycling of the encapsulated microcircuits induced large numbers of broken wires, but primarily only after extremely severe levels of stress. For MFR. C, both the TTL and CMOS parts showed broken wires at lower levels of stress, but all other device types survived until the final increment (2000 cycles from -65°C to +200°C) as seen in Figure 2-6. The reason for the differences between the various vendors is not understood - only MFR. E used a junction coat on the die. Note that MFR. A experienced only one failure while MFR. D experienced 25 failures in the final seve increment.

A comparison was made of the number of thermal cycling failures experienced on this program with epoxy encapsulated microcircuits using gold bonding wires, versus published data on numbers of comparable thermal cycling failures with hermetically sealed microcircuit using aluminum bonding wires. This comparison is shown in Figure 2-7. It is seen that the performance of the epoxy encapsulated microcircuits is comparable to or exceeds the performance of hermetic microcircuits using aluminum bond wires. In fact the results at -65°C to +200°C indicate that deformation of the encapsulant is probably not the cause of failure but merely normal expansion and contraction of the encapsulant causing the wires to work harden and break.

Hot intermittent opens (HIO) (open circuits observable only at elevated temperatures - in this case 125°C) were observed in 26 out of the 156 broken-wire failures. However this should not be cause for alarm, because HIOs were not observed in the bond failures, and in the case of broken wires, the temperature cycling environmental stress caused the failure rather than the measurement temperature.

2.2.4 Thermal Runaway

The Linear 741 Op Amp microcircuits failed in spectacular fashion while undergoing 1000 hour 150°C operating life test. 6 parts (12%) failed after only 144 hours, 3 parts (18% cumulative) after 168 hours, and 31 more parts (62% cumulative) after 672 hours as shown in Figure 2-8. These failures were violently catastrophic - the semiconductor die apparently failed in a short circuit mode which drew sufficient current from the power supplies to heat the epoxy encapsulant to the flame ignition point. Many of the devices had the encapsulant consumed so completely that only a white ash was left.

The test was stopped at 672 hours. Apparently it is not possible to operate these devices at 150°C without some form of circuit-by-circuit current limiting protection. This places a severe handicap on attempts to determine the extended life capabilities of the gold metallized linear microcircuits.

2.2.5 Stress Corrosion Cracking

The Manufacturer A parts experienced severe degradation of the external leads after the 175°C operating life test increment of Group 206. Metallurgical analysis showed the problem to be caused by stress corrosion cracking of the leads accompanied by severe breakage of the leads. The stress corrosion cracking was determined to be caused by chlorine present under the silver plating on the leads. It is postulated that an improper cleaning procedure resulted in inadequate removal of a chlorine-containing cleaning solution applied after the silver plating was applied. Wherever there were breaks in the silver plating, the chlorine attacked the Alloy 42 (iron-nickel) lead material causing transgranular cracks shown in Figures 2-9 and 2-10.

2.2.5 Stress Corrosion Cracking (Continued)

This occurrence of stress corrosion cracking at 175°C must be considered in procurement controls on encapsulated microcircuits, since it represents a good example of how an uncontrolled part type can demonstrate anomalous failure mechanisms. The activation energy of the stress corrosion cracking phenomenon is not known, hence it is not possible to extrapolate the observed 175°C failures down to normal system operating temperatures. However possibility of long term exposure to normal system operating temperatures causing stress corrosion cracking seems to exist, and precautions should be taken to avoid use of lots of parts which have latent stress corrosion cracking possibilities.

2.2.6 Ruptured Encapsulant

By the time the 200°C operating life test was ready to be performed, only three device types still survived: Manufacturer B, C, and D TTL. These parts completed the 1000 hour operating life test at 200°C, but universally suffered gross failures due to deformation and swelling of the encapsulant. It is not known exactly when this deformation occurred during the 1000 hour test. However C. H. Zierdt of Bell Telephone Labs has privately communicated the information that in his experience the epoxy encapsulant "lets go" after 800 hours at 200°C. Apparently at this temperature (25°C above the nominally specified glass transition temperature), the novolac encapsulant over-cures, changes state, or over-expands, causing the encapsulant material to split and crack. This violent deformation breaks lead wires loose inside the package causing failure.

The practical result of this finding is that a maximum upper limit for high stress testing of epoxy encapsulated microcircuits is +175°C.

2.2.7 Absorbed Moisture

Four failures occurred with CMOS devices that have been attributed to moisture absorbed during humidity cycling following thermal shock (Group 201). Three of these devices (Mfr. E) recovered to normal operation after bake out, and since no bias was previously applied, channeling is ruled out, leaving the conclusion that moisture absorbed by the encapsulant around the leads caused leakage currents to exceed the normal low CMOS circuit currents. The fourth device (Mfr. C) was found to have severe symptoms of electrical overstress. Again, since no bias had been applied previously, absorbed moisture is felt to be the cause of the destructive currents which occurred during electrical testing. None of the TTL or linear microcircuits showed any degradation due to humidity testing. This indicates that the low current regions of operation of CMOS parts cause them to be susceptible to moisture if it enters the package, and thus to be susceptible to combinations of thermal shock and humidity testing.

2.2.8 Cracked Die

Two incidences of cracked dice were observed in the program. One occurred in Group 202 after 2000 temperature cycles from -55°C to +125°C, and the other occurred at the end of Group 207, after 1000 temperature cycles from -55°C to +125°C, 2 days vacuum operating life, 1000 hours operating life at +5°C and 1000 hours operating life at +125°C. In both cases, the parts were Mfr. E parts which employ the junction overcoat for extra protection of the die surface. It was not possible to determine if these failures occurred as a direct result of the environmental stresses or if they pre-existed and were ultimately detected by the tri-temperature electrical testing.

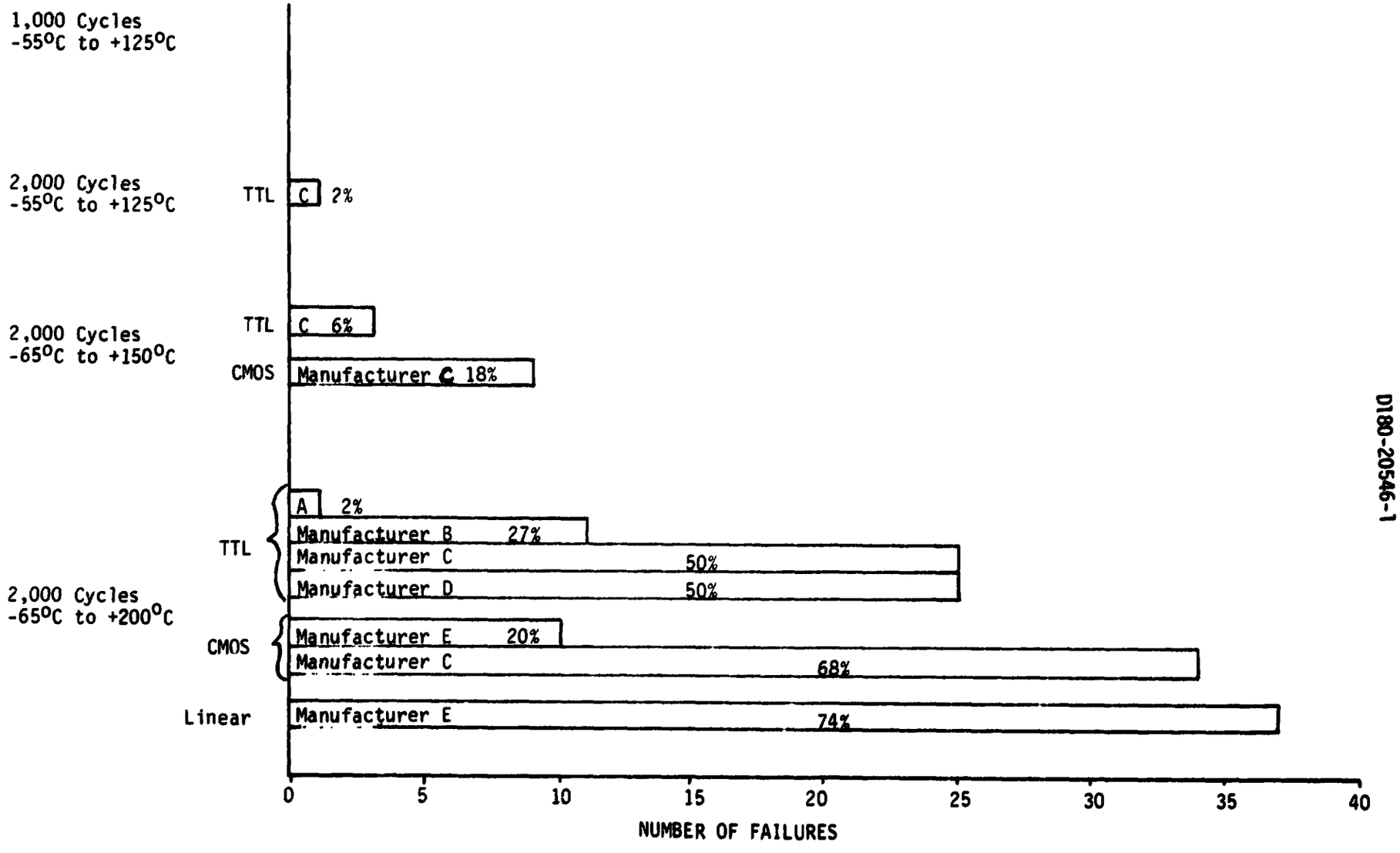


Figure 2-6. Summary of Temperature Cycling Broken Wire Failures

	NUMBER OF PART-CYCLES PER FAILURE		
	Condition B -55°C to +125°C	Condition C -65°C to +150°C	Condition D -65°C to +200°C
Hermetic Microcircuits with Aluminum Bond Wires (1) (1968)			2,780
Hermetic Microcircuit with Improved Aluminum Bond Wires (1) (1968)			24,000
Hermetic Op-Amp in TO-5 Can (3) (1970) (Aluminum Bond Wires)			1,669
Hermetic Microcircuits (2) (1974) (Aluminum Bond Wires)		10,600	12,500
Epoxy Encapsulated Microcircuits (1976)	700,000	58,300	4,900

Figure 2-7. Comparison of Hermetic Microcircuit Thermal Cycling Failures to Epoxy Encapsulated Microcircuit Failures

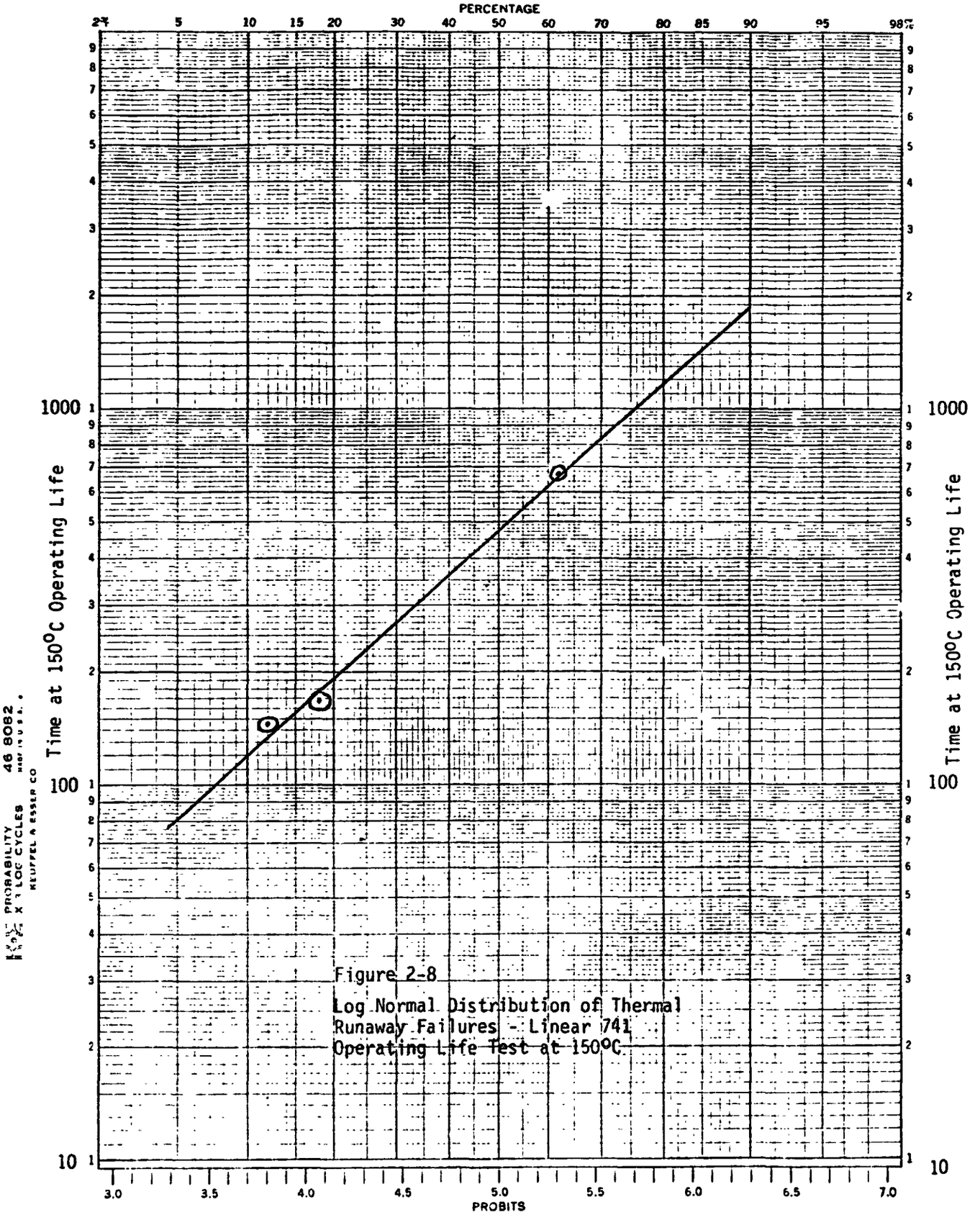


Figure 2-8

Log Normal Distribution of Thermal Runaway Failures - Linear 741 Operating Life Test at 150°C

100X

Figure 2-9. Stress Corrosion Cracking and Plating Degradation

250X

Figure 2-10. Close-up of Stress Corrosion Cracking at Site of Plating Rupture

2.3 Conclusions

Two major conclusions were derived from this program.

1. The TTT bipolar epoxy encapsulated microcircuits performed very well on this program. Although the data is somewhat limited because of small sample sizes, it appears that the digital TTL technology provides a very stable product in epoxy encapsulated form.

   Conversely, the CMOS devices demonstrated marked instability in epoxy encapsulated form, suffering from extensive channeling when subjected to elevated temperature life testing. It could not be conclusively shown that the epoxy encapsulant was or was not responsible for the channeling; however whatever the cause, the encapsulated CMOS devices appear to be much too unstable for reliable use in space applications and no further effort should be spent on evaluation of CMOS parts for space applications.

   The bipolar linear devices (gold metallized) did not perform flawlessly, suffering most dramatically from apparent thermal runaway. Thus the linear devices cannot presently be recommended for space applications but need additional testing to ascertain their true performance characteristics.

2. The two major advantages of encapsulated microcircuits - low cost and freedom from loose particles - appear to be readily transferable to space technology applications, at least for bipolar TTL devices. The loose particle problem is reduced to the lowest possible probability of occurrence by the use of encapsulated microcircuits. The cost advantage of encapsulated microcircuits shows potential for realization in space applications without introducing contradictory excessive screening costs, since the program results tended to show that three-temperature electrical measurement is the more important screen of the many various screens and environmental tests used in the program.

The following conclusions were derived concerning specific aspects of the program objectives.

Ineffective Screens on Stress Tests

The results of the environmental stress testing show that three of the environments used had no effect on device performance: vibration, vacuum operating life, and low temperature operating life. It is felt that these environments should not be considered further in investigation of the integrity of encapsulated microcircuits or in the development of screening and qualification tests for procurement of encapsulated microcircuits for space applications.

Thermal Cycling Stress Tests

The temperature cycling environmental stress testing caused failures in encapsulated microcircuits at a rate that is no worse than has been historically reported with hermetically sealed microcircuits that employ aluminum bond wires (see figure 2-7). As a result, it can be concluded that thermal cycling stress tests are of reduced importance in screening or qualifying encapsulated microcircuits for space applications. Periodic reassessment of the thermal cycling integrity of particular device types may be desirable as a precaution against possible new failure mechanisms introduced by new processing improvements, but universal use of thermal cycling as a 100% screen seems to be undesirable.

High Temperature Stress Tests

High temperature operating life tests were seen to be very effective in identifying failure mechanisms that might occur at usage temperatures. In particular, CMOS devices were found to be very susceptible to channeling, with high temperature operating life (150°C or even 175°C) seen as a valuable vehicle for identifying channeling trends.

The stress corrosion cracking failures observed in one manufacturer's parts also lends credence to the desirability of 175°C life tests: the acceleration of this mechanism at 175°C was very dramatic. While most manufacturers may be free from this problem, the uncontrolled nature of encapsulated microcircuit procurement leaves an area of vulnerability to improper processing that could cause stress corrosion cracking.

A small number of "plastic plague" gold-aluminum bond failures was observed at the 175°C operating life increment, which means that the trends toward gold-aluminum bond degradation can be determined readily by such a test.

The rupture of the epoxy encapsulant under 1000 hour 200°C operating life indicates that 175°C is an important upper limit on allowable temperature for extended stress testing. Beyond this temperature the Arrhenius relationship does not hold since the epoxy rapidly deteriorates.

The results of the program tend to indicate that the most advantageous screening test for encapsulated microcircuits is 100% electrical measurement at -55°C, 25°C, and +125°C. This conclusion is derived from the almost complete absence of diffusion shorts, bulk flaws, oxide shorts, and other die related failure mechanisms under the various conditions of high stress environmental testing. It appears that performing the tri-temperature (-55°C, 25°C, 125°C) electrical measurement just prior to the environmental stress tests eliminated all of the potential die-flaw failures. This trend should be verified by additional testing on large sample sizes, but the preliminary results show this premise to have some validity.

Recommended Screening Procedure

The recommended screening sequence for solid encapsulated microcircuits is to perform tri-temperature electrical measurements and then if urgently indicated, perform 160 hour burn-in at 125°C followed by tri-temperature electrical measurement. Stabilization bake, thermal cycling, and centrifuge should be avoided in the interests of reduced cost and improved device life time, and burn-in itself could be eliminated.

Recommended Qualification Procedure

Qualification tests recommended are high temperature operating life at 175°C preceded and followed by electrical measurement at all three temperatures. Qualification should be performed on each procurement lot to compensate for the continual and rapid changes in processing technologies that occur in commercial encapsulated microcircuits.

Constraints on Use of Encapsulated Microcircuits

Allowing for the limited sample sizes used on this program and the large time increment between electrical measurements, the indications are that there are no constraints on the use of TTL-technology encapsulated microcircuits in space environments as long as there is assurance that stress corrosion cracking is not a problem. More specifically designed tests should be performed on statistically significant sample sizes to verify the validity of the limited statistical evidence developed on this program. However for CMOS and linear devices certain constraints seem to apply. CMOS microcircuits should not be used at all because of potential channeling problems. Linear devices must be operated well within their rated junction temperatures to avoid problems of thermal runaway.

Advantages of Unique Processing or Packaging Technologies

The two unique processes used for devices tested on this program were a resin junction coat for one CMOS part type and gold die metallization on the linear part type. The only slight advantage observed was that the resin junction coat prevented deformation of the bond wires due to injection molding forces. However, this deformation was not a problem that caused confirmed failures of any parts. The gold die metallization did not cause any problems. The number of gold-aluminum bond failures in aluminum-die-metallized parts, was extremely small, and occurred primarily at the 175°C stress temperature to which the linear parts were never exposed. Thus any specific advantages of gold metallization could not be observed although theoretically there should be no problems of die bonds in the gold-to-gold metallurgical system.

3.0 TEST PROGRAM DESCRIPTION

The evaluation of solid encapsulated microcircuits was performed by conducting the following tasks: the required test parts were procured; construction analysis was performed on five devices of each of the seven part types; all parts received were screened to JAN Level B requirements (MIL-STD-883A, Method 5004.2); environmental stress tests were performed on 325 parts (survivors of screening) of each device type from each manufacturer; electrical measurement and data analysis was performed to identify failures at each stress increment; and failure analysis was performed on electrical failures. A flow diagram of the program is shown in Figure 3-1.

3.1 Parts Procurement

The TTL, CMOS, and Linear device types listed in Table 3-1 were procured in quantities of 500 each. This quantity was chosen to yield 325 parts after JAN Level B screening, plus five additional parts for construction analysis. The parts were procured from authorized distributor stocks with selection of the distributor based on lowest possible price. They were purely commercial grade parts and there was no knowledge of any prior screening tests performed by the manufacturers.

Table 3-1: Parts Procured

Mfr. Designation	Part Type	Device Type	Temperature Range Specified by Mfr.	Date Code
A	7400	TTL Quad 2-Input Nand Gate	0 to 100°C	7410
B	5400	TTL Quad 2-Input Nand Gate	-55 to 125°C	7407
C	5400	TTL Quad 2-Input Nand Gate	-55 to 125°C	508/511
D	7400	TTL Quad 2-Input Nand Gate	0 to 100°C	7425
E	4007	CMOS Dual Complementary Pair Plus Inverter	-40 to 85°C	444
C	4007	CMOS Dual Complementary Pair Plus Inverter	-40 to 85°C	446
E	741	Operational Amplifier	-55 to 125°C	527

As shown on the chart not all devices were designed to operate under the temperatures they were subjected to under the environmental stresses, as well as during electrical measurements. As a result of this, some MIL-M38510 electrical requirements were relaxed for parts unable to meet them.

3.2 Construction Analysis

The construction analysis procedure applied to five parts from each manufacturer were as follows:

(1) The parts were x-rayed in two planes in order to record (as well as could be accomplished with radiographic techniques) the relative position and dimensions of the leads and die.

(2) One part from each part type was sectioned longitudinally in order to record relative dimensions, observe, and record plating thicknesses, and inspect the die attach technique.

(3) Plastic was removed from die and lead frames of all parts not sectioned. (See paragraph 3.6 for techniques used.)

(4) The lead dress after stripping was recorded photographically and compared to that of the x-ray images to assure that plastic removal techniques were not distorting lead dress.

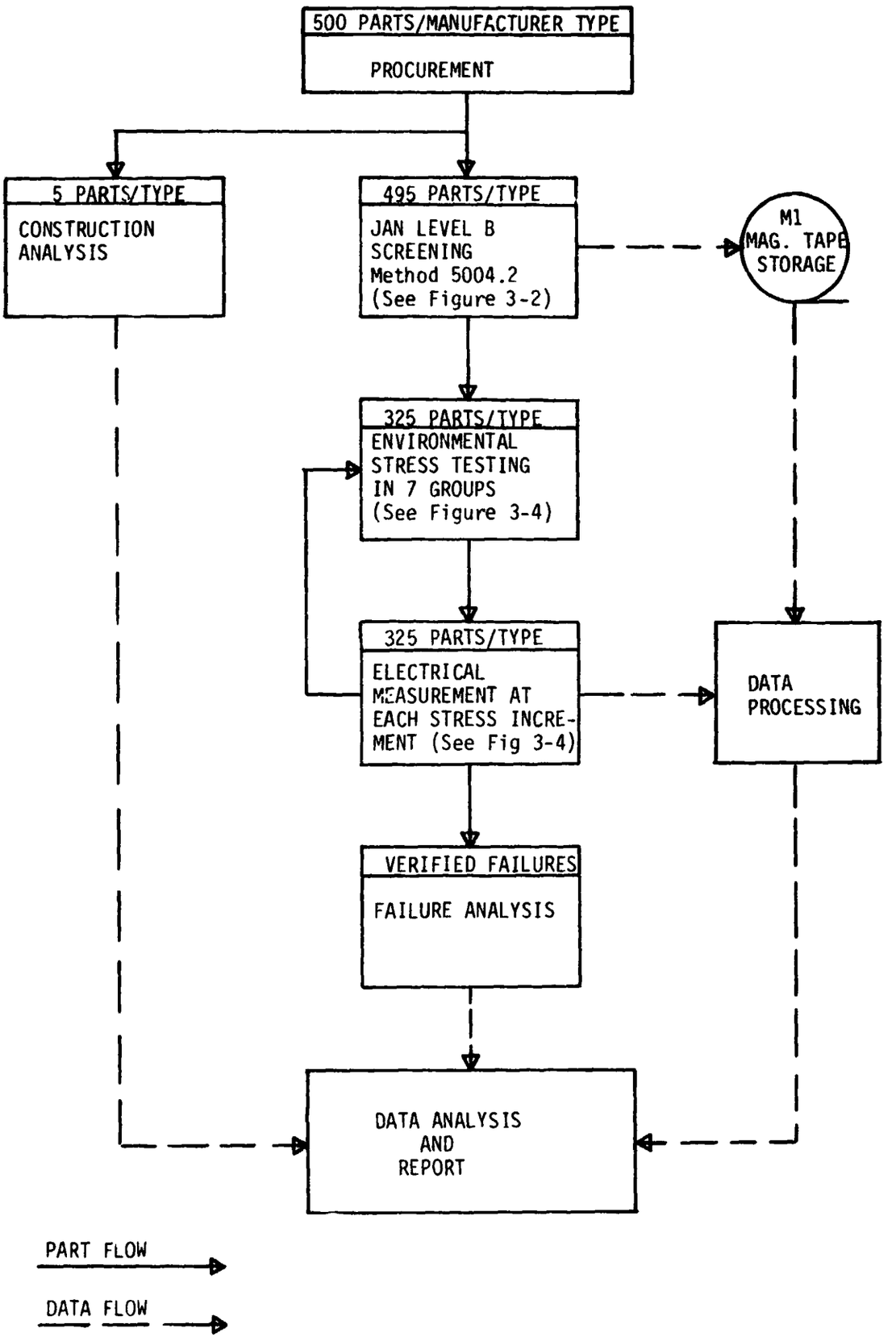


Figure 3-1. Solid Encapsulant Evaluation Flow

3.2 Construction Analysis (Continued)

(5) All parts were inspected (as well as plastic removal techniques would allow) for compliance with MIL-STD-883 (Method 2010.2) criteria. A typical die from each group of parts was photographed.

(6) One sample from each group of parts was inspected with a Scanning Electron Microscope, recording typical window coverage, bond shapes, die attach, and metal thickness.

(7) A bond pull test was performed on each bond from the remaining samples noting strength of pull and locations of wire/bond separation.

(8) A summary was prepared recording significant observations of the parts by different manufacturers. This includes a tabulation of encapsulant materials, materials used in the lead frames and platings, internal lead wire materials, chip metallizations, and die attach techniques.

Construction analysis results may be found in Appendix A.

3.3 Initial Screening

All parts with the exception of the construction analysis samples were subjected to screening in accordance with MIL-STD-883 Method 5004.2 Level B (excluding internal visual inspection and seal test) as shown in Figure 3-2.

Stabilization Bake: Method 1008.1 Condition C (24 hours @ 150°C)

The parts were stored at 150°C ± 2°C for 24 hours in an oven.

Temperature Cycling: Method 1010.1, Condition C (-65 to +150°C); 10 cycles, 20 minutes per cycle.

The parts were temperature cycled in a temperature chamber, automatically controlled to with ± 3°C. The temperature was monitored with a recorder to within ± 1°C. The parts were automatically transferred between the temperature cycler's two chambers. The separate chambers are independently charged with forced air heating (hot chamber) and forced blown liquid nitrogen cooling (cold chamber).

Constant Acceleration: Method 2001.1, Condition E (30,000 g, 1 minute).

Constant acceleration stress was provided by a high speed centrifuge. The parts were oriented with their tops outward so as to apply the acceleration force in the upward direction of the die relative to the lead frame.

Interim Electrical Parameters: MIL-M-38510, Group A, Subgroup 1, or relaxed equivalent.

The parts were measured at ambient room temperature with a computerized integrated circuit tester, and using stored measurement parameters. (See Tables 3-3, 3-4a, and 3-5 for parameters used.) For a complete discussion of electrical measurement techniques, see paragraph 3.5.

3.3 Initial Screening (Continued)

Burn In: Method 1015.1, 160 hours (min) @ 125°C.

Burn in tests were performed with the test devices mounted on specially designed and wired circuit boards. Figure 3-3 shows the circuit configuration used for the three device types. The boards were placed in the selected thermal environment chambers. Electrical voltage (and AC oscillator signals for the TTL devices) was applied gradually to design limits, and current was monitored to assure that proper power levels were established for each board. The chamber temperatures were raised to 125°C at a rate less than 75°C/minute, and were constantly recorded. The initial eight hours of life testing was observed by a test technician at 60 minute intervals, to insure test device safe power stabilization and chamber temperature stabilization.

Final Electrical Measurements

Within 96 hours after removal of the parts from burn in they were subjected to electrical measurements (as described in paragraph 3.5) according to MIL-M-38510 standards or relaxed equivalents. Electrical Parameters used are shown in Tables 3-3 through 3-5. These electrical measurements were stored on magnetic tape and used as the initial measurements (designated M1) with which all succeeding measurements were compared. Data from parts which failed at 25°C were analyzed to ensure that the failures were due to defects and not due to discrepancies between the MIL-spec parameter limits and the commercial part specification limits. Data from parts which failed at the temperature extremes was analyzed to ensure that they were truly nonfunctional failures and not just slight degradation of parameters as a result of testing the parts outside their design limit. The LTPD requirements of 5005.1 and the PDA requirements applied to subgroup 1, was not levied against the test sample, since it was not the intent of the screening program to accept or reject the lot, but rather to eliminate the devices unable to function after screening. The failures that occurred during pre-burn-in and post-burn-in screening are shown in Table 3-2.

External Visual

All surviving parts were subjected to visual examination to ensure compliance with the failure criteria listed in paragraph 3.1 of Method 2009.1, MIL-STD-883A.

Final Lot Identification

Of the parts surviving screening, 325 from each lot were identified as having "passed" (allowing for slight deviations as mentioned under "Final Electrical Measurement"), and were divided up into the necessary lots for subsequent environmental stress testing.

3.4 Environmental Stress Testing

Each manufacturer's parts were subjected to the stress testing program depicted in Figure 3-4. Electrical measurements per applicable M38510 slash sheets or relaxed equivalents were performed after each stress increment (see paragraph 3.5 for electrical measurement techniques). Series of tests were terminated for some part types when over 50% of the devices in those groups were identified as failures.

Manufacturer	Part Type	Initial Quantity of Parts	Pre Burn-In 25°C Electrical Measurement Failures	Post Burn-In Tri Temperature Electrical Measurement Failures (-55, 25, 125°C)	Final Yield	
					Number	Percent
A	7400 TTL	495	6	93	396	80%
B	5400 TTL	495	8	111	376	76%
C	5400 TTL	495	6	76	413	83%
D	7400 TTL	495	46	94	355	72%
E	4007 CMOS	495	59	101	335	68%
C	4007 CMOS	495	22	143	330	67%
E	741 Linear	495	15	154	326	66%

Table 3-2. Summary of Pre- and Post-Burn-In Failures

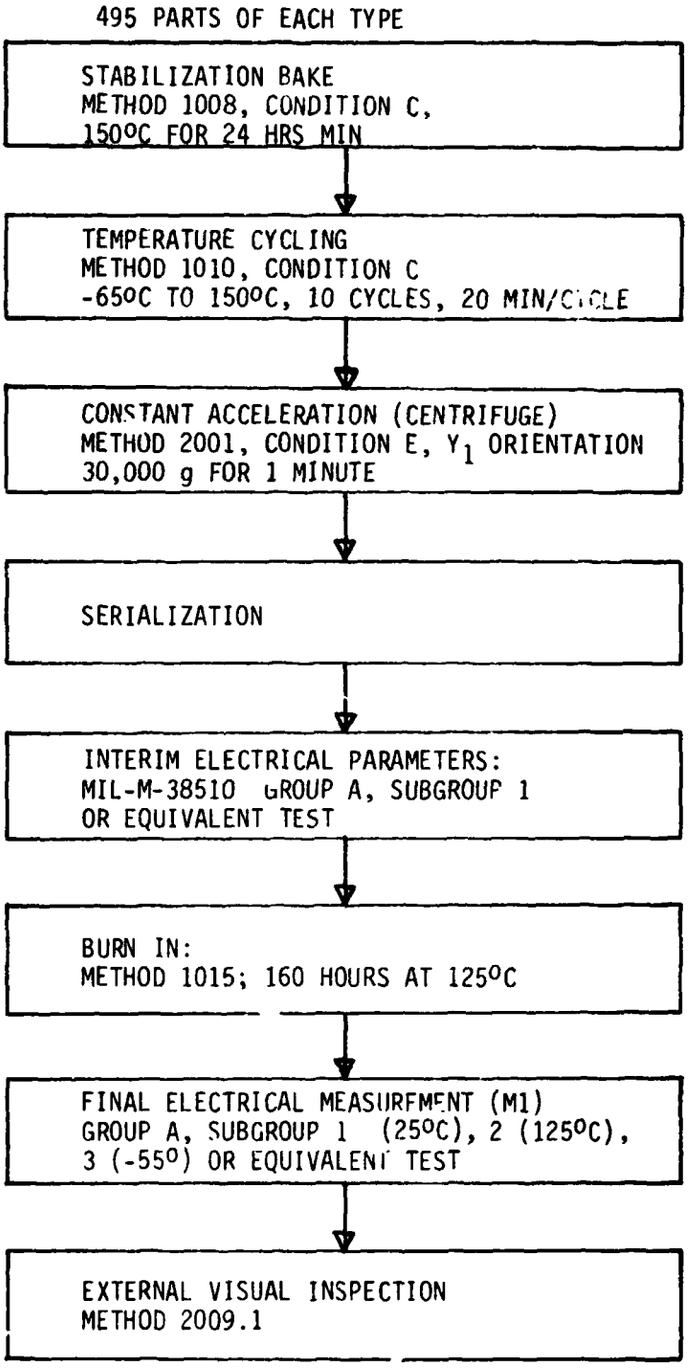


FIGURE 3-2. INITIAL SCREENING PER MIL-STD-883

D180-20546-1

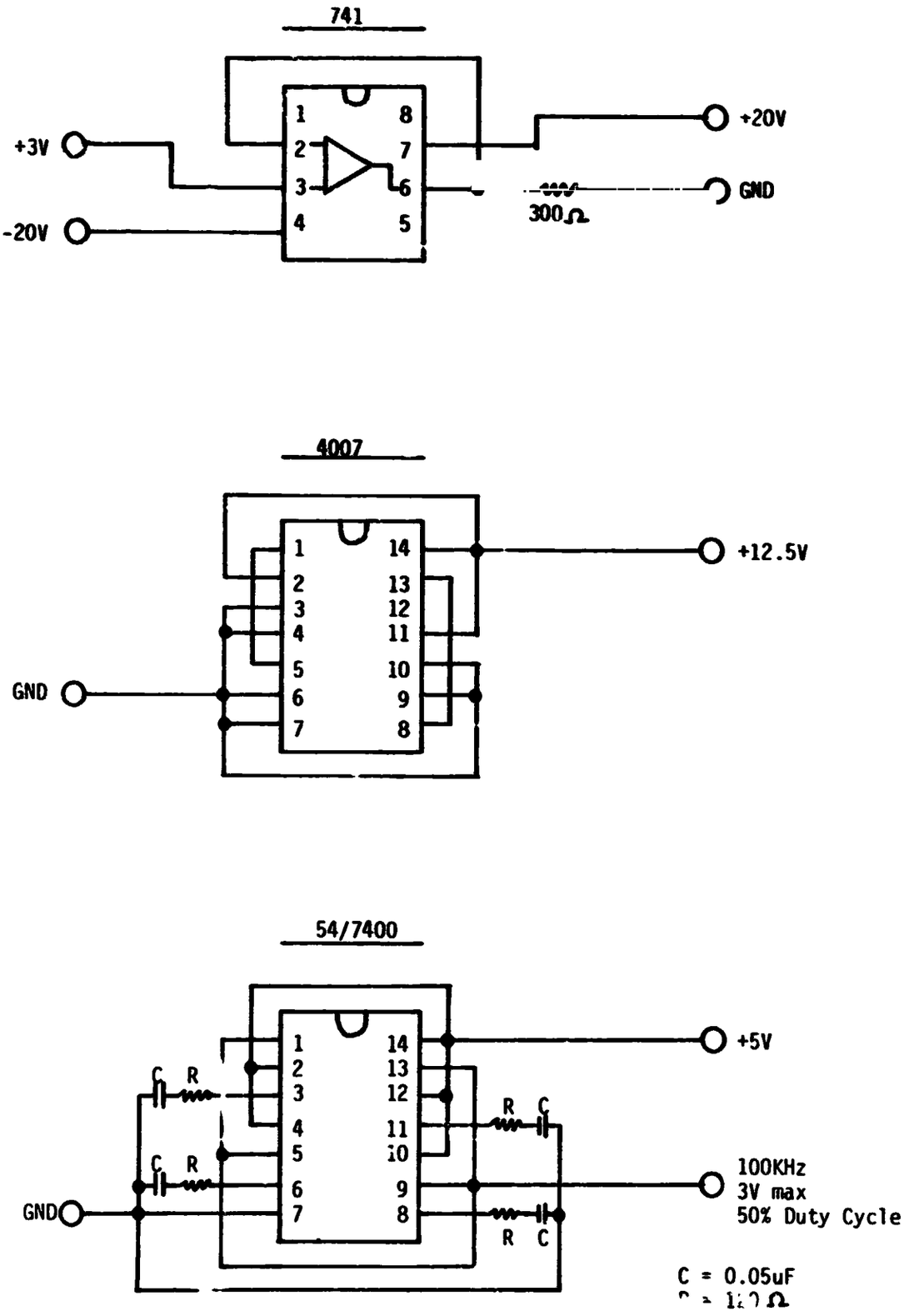


FIGURE 3-3: BURN IN AND OPERATING LIFE

TABLE 3-3. ELECTRICAL TEST PARAMETERS FOR 54/7400 DEVICES AT 25°C, 125°C, and -55°C PER MIL-M-38510/001-04

TEST NO.	TEST PARAMETER	CONDITIONS	LIMITS
1	Functional Test	Vcc = 4.5V	
2	Functional Test	Vcc = 4.5V	
3	Functional Test	Variable Vcc, 4.25V to 9.0V	
4	Functional Test	Variable Vcc, 2.5V to 9.0V	
5	Functional Test	Min. Input high, Vin = 2.4V	
6	Functional Test	Max. Input low, Vin = 0.8V	
7	Functional Test	Min. Gain $(V_{OH} - V_{OL})/(V_{IH} - V_{IL})$	
10	Functional Test	Min. Noise Immunity $V_{IH}(meas) - V_{IL}(max)$	
11	Functional Test	Min. Noise Immunity $V_{IL}(meas) - V_{IH}(min)$	
12	V_{OL} (1Y)	Vcc = 4.5V, Vin(A,B) = 2.0V	0.4V max
13	V_{OL} (2Y)	Vcc = 4.5V, Vin(A,B) = 2.0V	0.4V max
14	V_{OL} (3Y)	Vcc = 4.5V, Vin(A,B) = 2.0V	0.4V max
15	V_{OL} (4Y)	Vcc = 4.5V, Vin(A,B) = 2.0V	0.4V max
16	V_{OH} (1Y)	Vcc = 4.5V, Vin(A,B) @ 0.8V, 2.4V	2.4V min
17	V_{OH} (1Y)	Vcc = 4.5V, Vin(A,B) @ 2.4V, 0.8V	2.4V min
20	V_{OH} (2Y)	Vcc = 4.5V, Vin(A,B) @ 0.8V, 2.4V	2.4V min
21	V_{OH} (2Y)	Vcc = 4.5V, Vin(A,B) @ 2.4V, 0.8V	2.4V min
22	V_{OH} (3Y)	Vcc = 4.5V, Vin(A,B) @ 0.8V, 2.4V	2.4V min
23	V_{OH} (4Y)	Vcc = 4.5V, Vin(A,B) @ 2.4V, 0.8V	2.4V min
24	V_{OH} (4Y)	Vcc = 4.5V, Vin(A,B) @ 0.8V, 2.4V	2.4V min
25	V_{OH} (4Y)	Vcc = 4.5V, Vin(A,B) @ 2.4V, 0.8V	2.4V min
26	I_{OS} (1Y)	Vcc = 5.5V, Vin(A,B) = 0V	20mA min
27	I_{OS} (1Y)	Vcc = 5.5V, Vin(A,B) = 0V	55mA max
30	I_{OS} (2Y)	Vcc = 5.5V, Vin(A,B) = 0V	20mA min
31	I_{OS} (2Y)	Vcc = 5.5V, Vin(A,B) = 0V	55mA max
32	I_{OS} (3Y)	Vcc = 5.5V, Vin(A,B) = 0V	20mA min
33	I_{OS} (3Y)	Vcc = 5.5V, Vin(A,B) = 0V	55mA max
34	I_{OS} (4Y)	Vcc = 5.5V, Vin(A,B) = 0V	20mA min
35	I_{OS} (4Y)	Vcc = 5.5V, Vin(A,B) = 0V	55mA max
36	I_{IH1} (1A)	Vcc = 5.5V, Vin = 2.4V	40uA max
37	I_{IH2} (1A)	vcc = 5.5V, Vin = 5.5V	100uA max
40	I_{IL} (1A)	Vcc = 5.5V, Vin = 0.4V	0.7mA min
41	I_{IL} (1A)	Vcc = 5.5V, Vin = 0.4V	1.6mA max
42	I_{IH1} (1B)	Vcc = 5.5V, Vin = 2.4V	40uA max
43	I_{IH2} (1B)	Vcc = 5.5V, Vin = 5.5V	100uA max
44	I_{IL} (1B)	Vcc = 5.5V, Vin = 0.4V	0.7mA min
45	I_{IL} (1B)	Vcc = 5.5V, Vin = 0.4V	1.6mA max
46	I_{IH1} (2A)	Vcc = 5.5V, Vin = 2.4V	40uA max
47	I_{IH2} (2A)	Vcc = 5.5V, Vin = 5.5V	100uA max
50	I_{IL} (2A)	Vcc = 5.5V, Vin = 0.4V	0.7mA min
51	I_{IL} (2A)	Vcc = 5.5V, Vin = 0.4V	1.6mA max
52	I_{IH1} (2B)	Vcc = 5.5V, Vin = 2.4V	40uA max
53	I_{IH2} (2B)	Vcc = 5.5V, Vin = 5.5V	100uA max
54	I_{IL} (2B)	Vcc = 5.5V, Vin = 0.4V	0.7mA min
55	I_{IL} (2B)	Vcc = 5.5V, Vin = 0.4V	1.6mA max
56	I_{IH1} (3A)	Vcc = 5.5V, Vin = 2.4V	40uA max
57	I_{IH2} (3A)	Vcc = 5.5V, Vin = 5.5V	100uA max

TABLE 3-3. (Continued)

TEST NO.	TEST PARAMETER	CONDITIONS	LIMITS
60	I_{IL} (3A)	Vcc = 5.5V, Vin = 0.4V	0.7mA min
61	I_{IL} (3A)	Vcc = 5.5V, Vin = 0.4V	1.6mA max
62	I_{IH1} (3B)	Vcc = 5.5V, Vin = 2.4V	40uA max
63	I_{IH2} (3B)	Vcc = 5.5V, Vin = 5.5V	100uA max
64	I_{IL} (3B)	Vcc = 5.5V, Vin = 0.4V	0.7mA min
65	I_{IL} (3B)	Vcc = 5.5V, Vin = 0.4V	1.6mA max
66	I_{IH1} (4A)	Vcc = 5.5V, Vin = 2.4V	40uA max
67	I_{IH2} (4A)	Vcc = 5.5V, Vin = 5.5V	100uA max
70	I_{IL} (4A)	Vcc = 5.5V, Vin = 0.4V	0.7mA min
71	I_{IL} (4A)	Vcc = 5.5V, Vin = 0.4V	1.6mA max
72	I_{IH1} ( )	Vcc = 5.5V, Vin = 2.4V	40uA max
73	I_{IH2} (4B)	Vcc = 5.5V, Vin = 5.5V	100uA max
74	I_{IL} (4B)	Vcc = 5.5V, Vin = 0.4V	0.7mA min
75	I_{IL} (4B)	Vcc = 5.5V, Vin = 0.4V	1.6mA max
76	V_{IC} (1A)	Vcc = 4.5V, Iin = -12mA	-1.5V max
77	V_{IC} (1B)	Vcc = 4.5V, Iin = -12mA	-1.5V max
100	V_{IC} (2A)	Vcc = 4.5V, Iin = -12mA	-1.5V max
101	V_{IC} (2B)	Vcc = 4.5V, Iin = -12mA	-1.5V max
102	V_{IC} (3A)	Vcc = 4.5V, Iin = -12mA	-1.5V max
103	V_{IC} (3B)	Vcc = 4.5V, Iin = -12mA	-1.5V max
104	V_{IC} (4A)	Vcc = 4.5V, Iin = -12mA	-1.5V max
105	V_{IC} (4B)	Vcc = 4.5V, Iin = -12mA	-1.5V max
106	I_{CCL}	Vcc = 5.5V, Vin = 5.5V	*20mA max
107	I_{CCH}	Vcc = 5.5V, Vin = 0V	**6.6mA max

* Mfr. D - 22mA max, M38510/001 Limit = 5mA max.
** M38510/001 Limit = 1.65mA max.

TABLE 3-4a. ELECTRICAL TEST PARAMETERS FOR CMOS 4007 DEVICES PER MIL-M-38510/53-01 AT 25°C

TEST NO.	TEST PARAMETER	CONDITIONS	LIMITS
1	Functional Tests	V_{DD} = 4.5V	
2	Functional Tests	V_{DD} = 12.5V	
3	V_{IC} +(1A)	V_{DD} = 0V, I_{in} = 1mA	1.5V max
4	V_{IC} +(2A)	V_{DD} = 0V, I_{in} = 1mA	1.5V max
5	V_{IC} +(3A)	V_{DD} = 0V, I_{in} = 1mA	1.5V max
6	V_{IC} -(1A)	V_{SS} = 0V, I_{in} = -1mA	-6V max
7	V_{IC} -(2A)	V_{SS} = 0V, I_{in} = -1mA	-6V max
10	V_{IC} -(3A)	V_{SS} = 0V, I_{in} = -1mA	-6V max
11	I_{SS}	V_{IN} = 0V, V_{DD} = 15V	*2uA max
12	I_{SS}	V_{IN} = 15V, V_{DD} = 15V	*2uA max
13	V_{OH1} (1aY)	V_{IN} = 1.1V, I_{OH} = -.1mA, V_{DD} = 4.5V	2.5V min
14	V_{OH1} (2aY)	V_{IN} = 1.1V, I_{OH} = -.1mA, V_{DD} = 4.5V	2.5V min
15	V_{OH1} (3Y)	V_{IN} = 1.1V, I_{OH} = -.1mA, V_{DD} = 4.5V	2.5V min
24	V_{OH2} (1aY)	**V_{IN} = 1.1V, I_{OH} = -.75mA, V_{DD} = 5V	4.5V min
25	V_{OH2} (2aY)	**V_{IN} = 1.1V, I_{OH} = -.75mA, V_{DD} = 5V	4.5V min
26	V_{OH2} (3Y)	**V_{IN} = 1.1V, I_{OH} = -.75mA, V_{DD} = 5V	4.5V min
35	V_{OH3} (1aY)	V_{IN} = 1.1V, I_{OH} = 0, V_{DD} = 5V	4.95V min
36	V_{OH3} (2aY)	V_{IN} = 1.1V, I_{OH} = 0, V_{DD} = 5V	4.95V min
37	V_{OH3} (3Y)	V_{IN} = 1.1V, I_{OH} = 0, V_{DD} = 5V	4.95V min
46	V_{OH4} (1aY)	V_{IN} = 2.8V, I_{OH} = 0, V_{DD} = 12.5V	11.25V min
47	V_{OH4} (2aY)	V_{IN} = 2.8V, I_{OH} = 0, V_{DD} = 12.5V	11.25V min
50	V_{OH4} (3Y)	V_{IN} = 2.8V, I_{OH} = 0, V_{DD} = 12.5V	11.25V min
57	V_{OL1} (1aY)	V_{IN} = 3.8V, I_{OL} = 0.23mA, V_{DD} = 5.5V	0.4V max
60	V_{OL1} (2aY)	V_{IN} = 3.8V, I_{OL} = 0.23mA, V_{DD} = 5.5V	0.4V max
61	V_{OL1} (3Y)	V_{IN} = 3.8V, I_{OL} = 0.23mA, V_{DD} = 5.5V	0.4V max
70	V_{OL2} (1aY)	V_{IN} = 3.8V, I_{OL} = 0.6mA, V_{DD} = 5.0V	0.5V max
71	V_{OL2} (2aY)	V_{IN} = 3.8V, I_{OL} = 0.6mA, V_{DD} = 5.0V	0.5V max
72	V_{OL2} (3Y)	V_{IN} = 3.8V, I_{OL} = 0.6mA, V_{DD} = 5.0V	0.5V max
101	V_{OL3} (1aY)	V_{IN} = 3.8V, I_{OL} = 0, V_{DD} = 5.0V	50mV max
102	V_{OL3} (2aY)	V_{IN} = 3.8V, I_{OL} = 0, V_{DD} = 5.0V	50mV max
103	V_{OL3} (3Y)	V_{IN} = 3.8V, I_{OL} = 0, V_{DD} = 5.0V	50mV max
112	V_{OL4} (1aY)	V_{IN} = 9.5V, I_{OL} = 0, V_{DD} = 12.5V	1.25V max
113	V_{OL4} (2aY)	V_{IN} = 9.5V, I_{OL} = 0, V_{DD} = 12.5V	1.25V max
114	V_{OL4} (3Y)	V_{IN} = 9.5V, I_{OL} = 0, V_{DD} = 12.5V	1.25V max
123	I_{IH1} (1A,2A,3A)	V_{IN} = 15V, V_{DD} = 15V	3nA max
127	I_{IL1} (1A,2A,3A)	V_{IN} = 0V, V_{DD} = 15V	-3nA max

* M38510/53 Limit = 50nA max.
** Mfr. C Devices - I_{OH2} = -0.15mA.

TABLE 3-4b. ELECTRICAL TEST PARAMETERS FOR CMOS 4007 DEVICES PER MIL-M-38510/53-01 AT -55°C

TEST NO.	TEST PARAMETER	CONDITIONS	LIMITS
1	Functional Tests	V_{DD} = 4.5V	
2	Functional Tests	V_{DD} = 12.5V	
11	I_{SS}	V_{IN} = 0, V_{DD} = 15V	*2uA max
12	I_{SS}	V_{IN} = 15V, V_{DD} = 15V	*2uA max
21	V_{OH1} (1aY)	V_{IN} = 1.35V, I_{OH} = -0.1mA, V_{DD} = 4.5V	2.5V min
22	V_{OH1} (2aY)	V_{IN} = 1.35V, I_{OH} = -0.1mA, V_{DD} = 4.5V	2.5V min
23	V_{OH1} (3Y)	V_{IN} = 1.35V, I_{OH} = -0.1mA, V_{DD} = 4.5V	2.5V min
32	V_{OH2} (1aY)	**V_{IN} = 1.35V, I_{OH} = -0.15mA, V_{DD} = 5.0V	4.5V min
33	V_{OH2} (2aY)	**V_{IN} = 1.35V, I_{OH} = -0.15mA, V_{DD} = 5.0V	4.5V min
34	V_{OH2} (3Y)	**V_{IN} = 1.35V, I_{OH} = -0.15mA, V_{DD} = 5.0V	4.5V min
43	V_{OH3} (1aY)	V_{IN} = 1.35V, I_{OH} = 0, V_{DD} = 5.0V	4.95V min
44	V_{OH3} (2aY)	V_{IN} = 1.35V, I_{OH} = 0, V_{DD} = 5.0V	4.95V min
45	V_{OH3} (3Y)	V_{IN} = 1.35V, I_{OH} = 0, V_{DD} = 5.0V	4.95V min
54	V_{OH4} (1aY)	V_{IN} = 3.05V, I_{OH} = 0, V_{DD} = 12.5V	11.25V min
55	V_{OH4} (2aY)	V_{IN} = 3.05V, I_{OH} = 0, V_{DD} = 12.5V	11.25V min
56	V_{OH4} (3Y)	V_{IN} = 3.05V, I_{OH} = 0, V_{DD} = 12.5V	11.25V min
65	V_{OL1} (1aY)	V_{IN} = 3.95V, I_{OH} = 0, V_{DD} = 5.5V	0.4V max
66	V_{OL1} (2aY)	V_{IN} = 3.95V, I_{OH} = 0, V_{DD} = 5.5V	0.4V max
67	V_{OL1} (3Y)	V_{IN} = 3.95V, I_{OH} = 0, V_{DD} = 5.5V	0.4V max
76	V_{OL2} (1aY)	V_{IN} = 3.95V, I_{OH} = 0.75mA, V_{DD} = 5.0V	0.5V max
77	V_{OL2} (2aY)	V_{IN} = 3.95V, I_{OH} = 0.75mA, V_{DD} = 5.0V	0.5V max
100	V_{OL2} (3Y)	V_{IN} = 3.95V, I_{OH} = 0.75mA, V_{DD} = 5.0V	0.5V max
107	V_{OL3} (1aY)	V_{IN} = 3.95V, I_{OH} = 0, V_{DD} = 5.0V	50mV max
110	V_{OL3} (2aY)	V_{IN} = 3.95V, I_{OH} = 0, V_{DD} = 5.0V	50mV max
111	V_{OL3} (3Y)	V_{IN} = 3.95V, I_{OH} = 0, V_{DD} = 5.0V	50mV max
120	V_{OL4} (1aY)	V_{IN} = 9.75V, I_{OH} = 0, V_{DD} = 12.5V	1.25V max
121	V_{OL4} (2aY)	V_{IN} = 9.75V, I_{OH} = 0, V_{DD} = 12.5V	1.25V max
122	V_{OL4} (3Y)	V_{IN} = 9.75V, I_{OH} = 0, V_{DD} = 12.5V	1.25V max

* M38510/053 Limit = 50nA max.
** M38510/053 I_{OH2} = -0.95mA.

TABLE 3-4c. ELECTRICAL TEST PARAMETERS FOR CMOS 4007 DEVICES PER MIL-M-38510/53-01 AT 125°C

TEST NO.	TEST PARAMETERS		CONDITIONS	LIMITS
1	Functional Tests		V_{DD} = 4.5V	
2	Functional Tests		V_{DD} = 12.5V	
11	I_{SS}		V_{IN} = 0V, V_{DD} = 15V	*2uA max
12	I_{SS}		V_{IN} = 15V, V_{DD} = 15V	*2uA max
16	V_{OH1} (1a)		V_{IN} = 0.85V, I_{OH} = -0.1mA, V_{DD} = 4.5V	2.5V min
17	V_{OH1} (2a)		V_{IN} = 0.85V, I_{OH} = -0.1mA, V_{DD} = 4.5V	2.5V min
20	V_{OH1} (3Y)		V_{IN} = 0.85V, I_{OH} = -0.1mA, V_{DD} = 4.5V	2.5V min
27	V_{OH2} (1aY)	**	V_{IN} = 0.85V, I_{OH} = -0.55 mA, V_{DD} = 5.0V	4.5V min
30	V_{OH2} (2aY)	**	V_{IN} = 0.85V, I_{OH} = -0.55 mA, V_{DD} = 5.0V	4.5V min
31	V_{OH2} (3Y)	**	V_{IN} = 0.85V, I_{OH} = -0.55 mA, V_{DD} = 5.0V	4.5V min
40	V_{OH3} (1aY)		V_{IN} = 0.85V, I_{OH} = 0, V_{DD} = 5.0V	4.95V min
41	V_{OH3} (2aY)		V_{IN} = 0.85V, I_{OH} = 0, V_{DD} = 5.0V	4.95V min
42	V_{OH3} (3Y)		V_{IN} = 0.85V, I_{OH} = 0, V_{DD} = 5.0V	4.95V min
51	V_{OH4} (1aY)		V_{IN} = 2.55V, I_{OH} = 0, V_{DD} = 12.5V	11.25V min
52	V_{OH4} (2aY)		V_{IN} = 2.55V, I_{OH} = 0, V_{DD} = 12.5V	11.25V min
53	V_{OH4} (3Y)		V_{IN} = 2.55V, I_{OH} = 0, V_{DD} = 12.5V	11.25V min
62	V_{OL1} (1aY)		V_{IN} = 3.6V, I_{OH} = 0.23mA, V_{DD} = 5.5V	0.5V max
63	V_{OL1} (2aY)		V_{IN} = 3.6V, I_{OH} = 0.23mA, V_{DD} = 5.5V	0.5V max
64	V_{OL1} (3Y)		V_{IN} = 3.6V, I_{OH} = 0.23mA, V_{DD} = 5.5V	0.5V max
73	V_{OL2} (1aY)		V_{IN} = 3.6V, I_{OH} = 0.4mA, V_{DD} = 5.0V	0.5V max
74	V_{OL2} (2aY)		V_{IN} = 3.6V, I_{OH} = 0.4mA, V_{DD} = 5.0V	0.5V max
75	V_{OL2} (3Y)		V_{IN} = 3.6V, I_{OH} = 0.4mA, V_{DD} = 5.0V	0.5V max
104	V_{OL3} (1aY)		V_{IN} = 3.6V, I_{OH} = 0, V_{DD} = 5.0V	50mV max
105	V_{OL3} (2aY)		V_{IN} = 3.6V, I_{OH} = 0, V_{DD} = 5.0V	50mV max
106	V_{OL3} (3Y)		V_{IN} = 3.6V, I_{OH} = 0, V_{DD} = 5.0V	50mV max
115	V_{OL4} (1aY)		V_{IN} = 3.6V, I_{OH} = 0, V_{DD} = 12.5V	1.25V max
116	V_{OL4} (2aY)		V_{IN} = 3.6V, I_{OH} = 0, V_{DD} = 12.5V	1.25V max
117	V_{OL4} (3Y)		V_{IN} = 3.6V, I_{OH} = 0, V_{DD} = 12.5V	1.25V max
124	I_{IH2} (1A)		V_{IN} = 15V, V_{DD} = 15V	45nA max
125	I_{IH2} (2A)		V_{IN} = 15V, V_{DD} = 15V	45nA max
126	I_{IH2} (3A)		V_{IN} = 15V, V_{DD} = 15V	45nA max
130	I_{IL2} (1A)		V_{IN} = 0V, V_{DD} = 15V	-45nA max
131	I_{IL2} (2A)		V_{IN} = 0V, V_{DD} = 15V	-45nA max
132	I_{IL2} (3A)		V_{IN} = 0V, V_{DD} = 15V	-45nA max

* M38510/53 Limit - 50nA max.
** Mfr. C Devices - I_{OH2} = -0.15mA.

TABLE 3-5. ELECTRICAL TEST PARAMETERS FOR LINEAR 741 DEVICES AT 25°C, 125°C, and -55°C

TEST NO.	TEST PARAMETER	CONDITIONS (V+ = + 15V)	LIMITS*
1	Gain	Closed Loop, V_O = -10V	-10V ± 1V
2	Gain	Closed Loop, V_O = +10V	+10V ± 1V
3	V_{os}		±7.5mV max
4	I_{os}		±1uA max
5	I_{IB}		±800nA max
6	+PSRR	Disturb Vcc+	77db
7	-PSRR	Disturb Vcc-	77db
10	CMRR		70db
11	CMVR		7.5mV max
12	$-V_{out}$ Swing	V = ±15V	-10V min
13	$+V_{out}$ Swing	V = ±15V	+10V min
14	A_{VOL}	Open Loop	14,925 min
15	Icc		3.6mA min
16	Pd		43mW max

* NOTE: Test limits are modified commercial 741 limits.

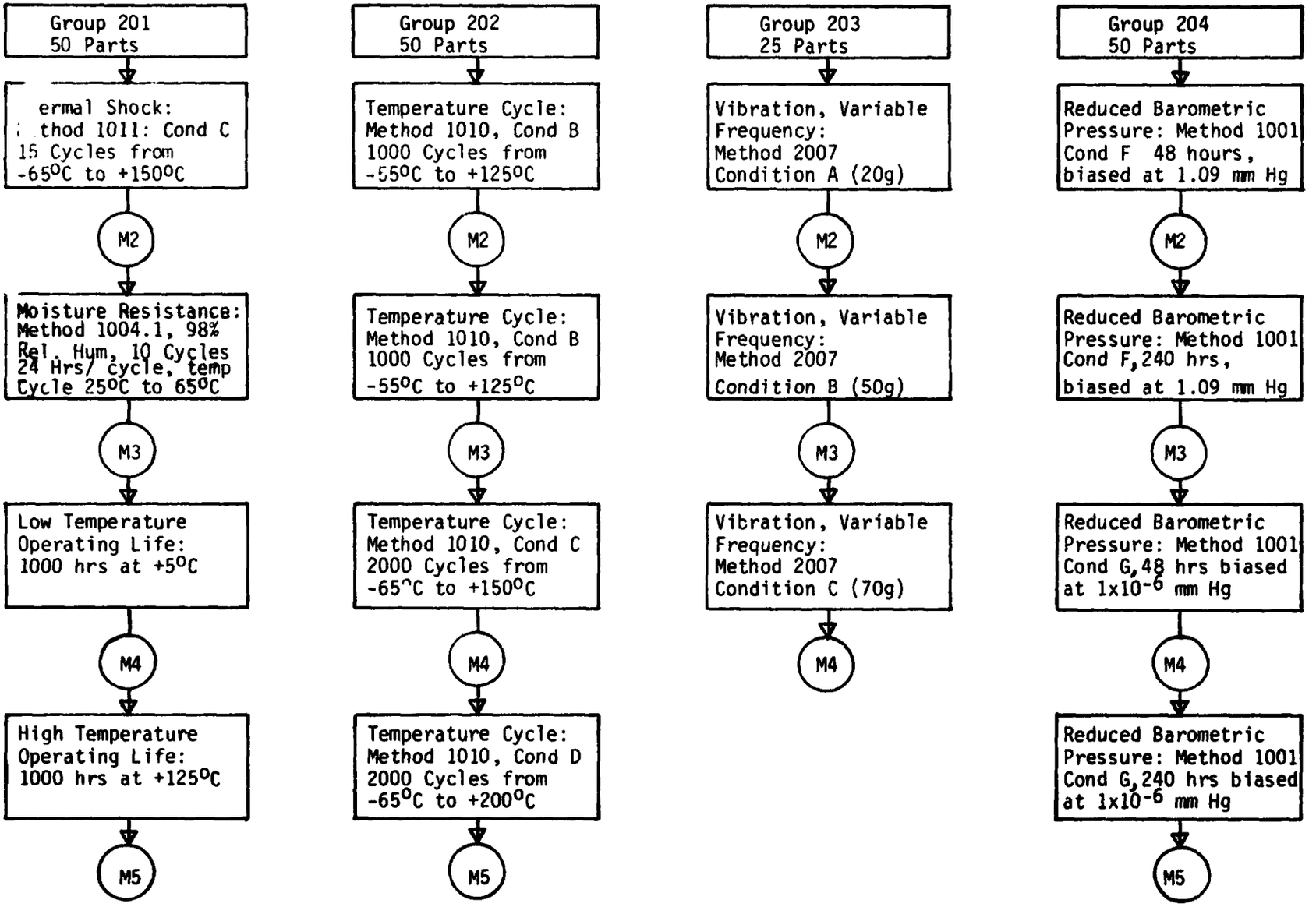


Figure 3-4a. Environmental Stress Test Flow (M(x) = Electrical Measurement at 25, -55, and 125°C)

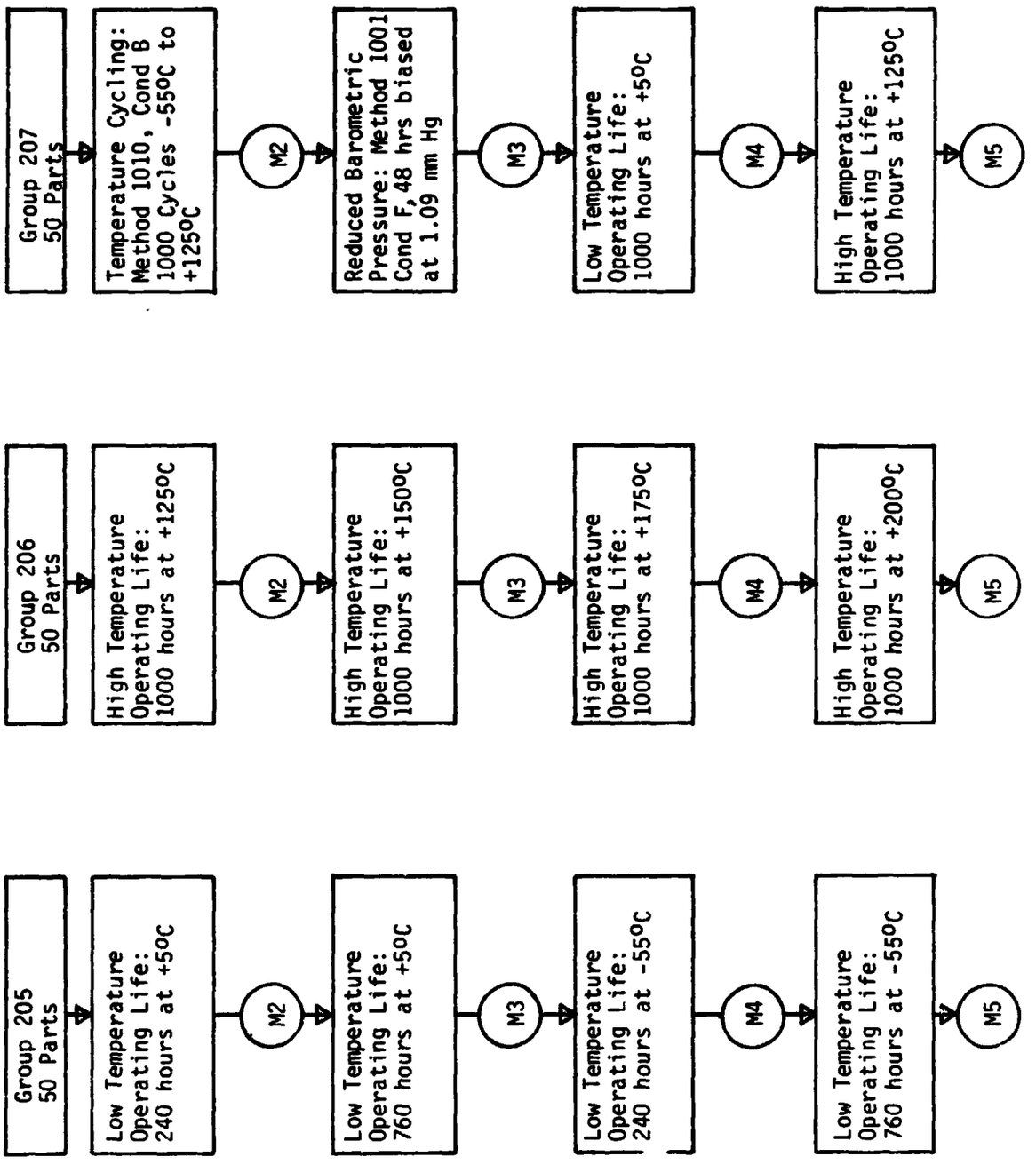


Figure 3-4b: Environmental Stress Test Flow (M(x) = Electrical Measurement at 25, -55, and 125°C)

3.4 Environmental Stress Testing (Continued)

Thermal Shock: Method 1011.1, Condition C: -65°C to +150°C, liquid to liquid, 15 cycles.

Thermal shock tests were performed in a Boeing apparatus consisting of two liquid baths maintained at 150°C (FC 48) and -65°C (FC 78). The parts were placed in a wire basket which was manually transferred from one bath to the other within 10 seconds and held in the baths for a minimum of 5 minutes. The hot temperature was controlled to within +5, -0°C, and the cold temperature to within +0, -5°C.

Moisture Resistance: Method 1004.1, 98% Relative Humidity, 10 continuous cycles, 24 Hours/cycle, temperature cycled 25°C to 65°C.

The moisture resistance tests were performed in a cam programmable humidity cabinet. The cabinet was programmed to provide the temperature/humidity profile shown in Figure 1004-1 of MIL-STD-883A.

Low Temperature Operating Life Tests: +5°C or -55°C.

The parts were inserted in burn in boards and installed and operated in temperature controlled chambers as described under Paragraph 3.3 "Burn in", except the temperatures were either +5°C (for 240, 760, or 1,000 hours) or -55°C (for 240, or 760 hours)

High Temperature Operating Life: 125, 150, 175, or 200°C for 1000 hours.

The parts were installed as above, the temperature chamber was adjusted to either 125, 150, 175, or 200°C, and were operated for 1,000 hours.

Temperature Cycling: Method 1010, Condition B (-55 to 125°C), Condition C (-65 to 150°C), or Condition D (-65 to 200°C) for either 1000 or 2000 cycles.

These tests were performed as described earlier under paragraph 3.3, except that because of the large numbers of cycles requiring unattended operation, additional precautions were taken. The recorder was observed by a test engineer for six cycles and the cycler fine tuned to within $\pm$ 1°C and $\pm$ 3 minutes. The temperature cycler was then monitored for the first 8 hours to ensure cycle repeatability and monitored once per working day thereafter.

Vibration, Variable Frequency: Method 2007, Condition A (20g), B (50g), or C (70g).

The variable frequency vibration test was accomplished by casting the leads of the parts in plates of Rigidax, a low temperature remeltable potting compound, and mounting the plates in a three sided cube fixture. The fixture was bolted to a vibration system and swept from 20 Hz to 2,000 Hz and back to 20 Hz in not less than 4 minutes, with a total of four sweeps in each direction (x, y, z). The appropriate force was established by monitoring an accelerometer attached to the vibration system.

3.4 Environmental Stress Testing (Continued)

Reduced Barometric Pressure: Method 1001, Condition F (1.09mmHg) or Condition G (2.4×10^{-6}mmHg), 48 or 240 hours.

The devices were mounted in sockets on boards (see Figure 3-3 for circuits used) connected to monitor circuitry capable of detecting arc-over or corona currents from DC to 30 mHz. They were then placed in a diffusion pump system and exposed to 48 or 240 hours of either 1.09 mmHg or 2.4×10^{-6} mmHg.

3.5 Electrical Testing and Data Processing Techniques

Electrical measurements and data manipulations were performed using a Teradyne J-283 computerized integrated circuit test system. MIL-M-38510 test programs (or modified equivalents) were assembled for each type of device and stored on magnetic tape. Tables 3-2, 3-3, and 3-4 list test parameters used for the TTL, CMOS, and Linear devices. When starting electrical testing, the appropriate test program was stored in computer memory. The device under test was placed in the test socket and stabilized at either 25°C, 125°C, or -55°C. Room temperature was used to accomplish 25°C testing. For testing at the temperature extremes (-55°C and 125°) a Thermostream System was used. The Thermostream tube was placed over the part and test socket, the desired temperature was selected, and electrical testing was initiated 30 seconds after temperature stabilization. The test system, using the stored test parameters, automatically tested the part, and stored the electrical measurements on magnetic tape. Parts which failed electrical testing were retested to confirm failure. Parts which failed catastrophically were removed from testing, and representative samples were subjected to failure analysis (see paragraph 3-6 for failure analysis procedures). Parts which failed only marginally were returned to testing. Data processing was accomplished by using the initial measurements (MI-stored during initial screening), the final electrical measurements, and computer processing capabilities to generate several types of output. Figure 3-5 is an example of the electrical measurement output for one Mfr. D device. Figure 3-6 is an output for one parameter of a group of Mfr. D devices showing the spread of parameter values for the group. Figure 3-7 is an output for the same group of Mfr. D devices showing the delta value spread for the same parameter. These types of outputs were used to monitor any significant effects of the environmental stress testing program on various electrical parameters of the plastic encapsulated devices.

3.6 Failure Analysis Procedures

Parts which were determined to be catastrophic failures during electrical testing, or representative samples of such parts, were subjected to failure analysis. The basic steps followed prior to dissection of the parts were as follows:

1. The environment history of the parts were studied to enable understanding of the various possible causes of failure.

A B C D E F G H I

1608 MX 1 +25C
1608 MX 1 7400 M4 LOT#201025 C 5-26-76

3	9.00	V	4	3.89	V	5	1.51	V	6	1.21	V
3	9.00	V	4	3.90	V	5	1.50	V	6	1.20	V
3	.00	V	4	.01	V	5	- .01	V	6	- .01	V
3	.0	%	4	.0	%	5	- .0	%	6	- .0	%
7	6.66	V	10	.89	V	11	.81	V	12	.227	V
7	6.65	V	10	.90	V	11	.80	V	12	.226	V
7	.00	V	10	.01	V	11	- .01	V	12	- .001	V
7	.0	%	10	1.0	%	11	- 1.0	%	12	- .0	%
13	.220	V	14	.221	V	15	.222	V	16	2.62	V
13	.217	V	14	.220	V	15	.220	V	16	2.71	V
13	- .003	V	14	- .001	V	15	- .002	V	16	.09	V
13	- 1.0	V	14	- .0	%	15	- .0	%	16	3.0	%
17	2.61	V	20	2.64	V	21	2.65	V	22	2.66	V
17	2.73	V	20	2.69	V	21	2.69	V	22	2.65	V
17	.12	V	20	.05	V	21	.04	V	22	- .01	V
17	4.0	%	20	1.0	%	21	1.0	%	22	- .0	%

A - Device Serial Number
B - Date
C - Electrical Measurement Number
D - Lot Number showing the group (201) and the temperature the device was measured at (25°C)
E - Test Parameter Number
F - Initial Measurement Value (M1 Value)
G - Final Measurement Value (M4 Value)
H - Delta Value (Final Value - Initial Value)
I - Percentage Change of Measured Value

Figure 3-5. Electrical Measurement Output For One Manufacturer D TTL Device

TEST NO. 43 7400 M4 LOT#201025 C 5-26-76

CELL WIDTH .2 UA
OF UNITS 49 ← Number of Devices in Group

10.0% PT.	2.8 UA
15.9% PT.	3.2 UA
MEDIAN	6.1 UA
84.1% PT.	16.4 UA
90.0% PT.	17.3 UA
MEAN	8.60 UA
SIGMA	6.00 UA

VALUE	CUM. %	CELL %	CELL #
1.6 UA	4.08%	4.08%	2
2.6 UA	8.16%	4.08%	2
2.8 UA	10.20%	2.04%	1
3.4 UA	18.37%	8.16%	4
3.6 UA	20.41%	2.04%	1
4.4 UA	28.57%	8.16%	4
4.6 UA	36.73%	8.16%	4
5.0 UA	38.78%	2.04%	1
5.2 UA	42.86%	4.08%	2
5.4 UA	46.94%	4.08%	2
6.0 UA	48.98%	2.04%	1
6.2 UA	53.06%	4.08%	2
6.4 UA	59.18%	6.12%	3
7.0 UA	61.22%	2.04%	1
7.2 UA	63.27%	2.04%	1
8.4 UA	65.31%	2.04%	1
10.4 UA	67.35%	2.04%	1
10.6 UA	71.43%	4.08%	2
11.6 UA	73.47%	2.04%	1
12.0 UA	75.51%	2.04%	1
13.6 UA	77.55%	2.04%	1
14.4 UA	79.59%	2.04%	1
16.2 UA	83.67%	4.08%	2
17.0 UA	85.71%	2.04%	1
17.2 UA	89.80%	4.08%	2
18.4 UA	91.84%	2.04%	1
19.2 UA	93.88%	2.04%	1
22.0 UA	95.92%	2.04%	1
22.2 UA	100.00%	4.08%	2

← Number of Devices in Group With I_{IH2} (1B) Values in 0.2uA Cell Ending With 1.6uA

Figure 3-6. Parameter Spread Output For a Group of Manufacturer D TTL Devices

TEST NO. 43 D 7400 M4 LOT#201025 C 5-26-7[illegible]

CELL WIDTH	.1 UA
# OF UNITS	49
10.0% PT. -	.1 UA
15.9% PT.	0 A
MEDIAN	.1 UA
84.1% PT.	.5 UA
90.0% PT.	.5 UA
MEAN	200. NA
SIGMA	300. NA

VALUE	CUM. %	CELL %	CELL #
- .9 UA	2.04%	2.04%	1
- .2 UA	4.08%	2.04%	1
0 A	18.37%	14.29%	7
.1 UA	53.06%	34.69%	17
.2 UA	61.22%	8.16%	4
.3 UA	75.51%	14.29%	7
.5 UA	85.71%	10.20%	5
.6 UA	97.96%	12.24%	6
.7 UA	100.00%	2.04%	1

← Number of Devices in Group With Delta Values in 0.1uA Cell Ending With -0.9uA

Figure 3-7. Parameter Delta Spread Output For a Group of Manufacturer D TTL Devices

2. The parts were electrically tested to verify the failure. This involved either bench testing or automatic testing of the parts, sometimes requiring environments comparable to those at which they failed, checking all significant parameters to ensure results similar to original test failures. Following confirmation of failures, careful pin to pin curve tracer measurements were made to localize or characterize the faults as well as possible.

3. Thorough exterior examinations, aided by microscopes, were conducted to preclude the possibility of external faults causing failure.

4. When channeling was suspected (as a product of the electrical characterization), the technique applied was high temperature storage of varying times and temperatures (up to 22 hours @ 175°C, and up to 300 hours at 150°C), followed by electrical testing. If self repair was evident following high temperature storage, channeling was inferred as the cause of failure.

Dissection Techniques:

The dissection technique most frequently employed involved using emory paper sanding drums (¼ inch diameter) to grind away an area directly above the die to a depth such that the leads were not disturbed. A frame was soldered to the external leads to provide a solid holder and the entire assembly was dipped for about 30 seconds in hot nitric acid (a 90% solution). For resin coated dice a 5-second exposure to nitric acid and a 30-second exposure to hot sulfuric acid was used. The acid removed the epoxy evenly at all points, but exposed the die before totally exposing the lead frame. For both nitric and sulfuric acids, only acetone was employed as a rinse, since water would have caused excessive metallization damage. Another dissection technique infrequently employed was to use an acid resistant cement to coat the leads and package (except directly above the die) prior to acid exposure. Although these techniques worked well to expose the die and leads, entire removal of epoxy without damaging the die or lead frame was sometimes difficult if not impossible. This was particularly true of devices which for various reasons had shorted junctions or burned metallizations. In most cases though, epoxy removal was sufficient to enable identification of failure causes.

Following dissection of the parts, autopsy efforts proceeded using standard techniques such as visual inspection, micro-manipulator probing, and SEM examinations. Bond pulling, die shearing, metallurgical sectioning, and other destructive tests were performed as needed to provide supplemental information. Failure causes were identified and documented, and succeeding failures were analyzed to the point required to provide a high degree of confidence that the same failure cause as previously documented was repeated.

4.0 TEST RESULTS AND DISCUSSION

4.1 Summary of Results

Figures 4-1 through 4-7 summarize the valid failures that occurred as a result of the environmental stress testing. The valid failures that occurred were found to be due to several predominant causes:

- o channeling of CMOS devices due to operating life test at elevated temperatures
- o broken lead wires due to extremely severe temperature cycling
- o Gold-aluminum intermetallics at the ball-bond-to-aluminum interface due to operating life test at elevated temperatures
- o Gross deformation and swelling of the plastic encapsulant due to life test at 200°C.
- o Stress Corrosion Cracking

Other isolated failure mechanisms were observed in small quantities for specific cases. These probably represent normal freak failure mechanisms present in any group of basically cheap commercial parts.

4.2 Stress Tests That Resulted in No Valid Failures

As seen by Figures 4-3, 4-4, and 4-5, three of the environmental stress groups (203, 204, 205) resulted in no valid failures at all. There were a number of device failures due to operating-life-test-board/socket malfunctions. These failures are not considered valid but are classified as abuse failures. Thus it can be concluded that the three environments represented by these groups (203: vibration; 204: Vacuum Operating Life; 205: Low Temperature Operating Life) are totally ineffective in generating failure data for TTL, CMOS, or gold linear encapsulated microcircuits. As a further conclusion, these tests or environments would be ineffective as qualification tests or acceptance screen tests, even for parts to be used in a low temperature, high vacuum space environment.

4.3 Stress Tests that Caused Failures

Four out of the seven environmental test groups (201, 202, 206, 207) experienced failures that are considered valid failures, although the failure mode is not attributable to the particular stress in all cases. A discussion will be made of the results from each of the four groups, followed by an overall summary of the interrelationships.

4.3.1 Group 201 Test Results

This group received the following environmental stresses

15 cycles of Thermal Shock from -65°C to +150°C
M2
Moisture Resistance: 10 days per MIL-STD-883
M3
1000 hour Operating Life at +5°C
M4
1000 hour Operating Life at +125°C
M5

		TTL				CMOS		Gold Linear
Measurement Number	Previous Environment	Mfr. A 7400	Mfr. B 5400	Mfr. C 5400	Mfr. D 7400	Mfr. E 4007	Mfr. C 4007	Mfr. E 741
M2	Thermal Shock: 15 cycles from -65°C to +150°C							
M3	Moisture Resistance 10 day @ 98% RH 25°C cycled to 65°C				1 Lifted bond plague	3 Absorbed moisture	1 Absorbed moisture	
M4	1000 hour Operating Life @ +75°C							
M5	1000 hour Operating Life @ +125°C					6 n-FET channeling	24 n-FET channeling	

Figure 4-1. Group 201 Failure Summary: Number Failed Out of Each Group of 50 Parts

		TTL				CMOS		Gold Linear
Measurement Number	Previous Environment	Mfr. A 7400	Mfr. B 5400	Mfr. C 5400	Mfr. D 7400	Mfr. E 4007	Mfr. C 4007	Mfr. E 741
M2	1000 Temp. Cycles -55°C to +125°C							
M3	1000 Temp. Cycles -55°C to +125°C (total of 2000 cycles)			1 Broken wires		2 (1) Peri-pheral open ball bond (1) Cracked die		
M4	2000 Temp. Cycles -65°C to +150°C			3 Broken wires			9 Broken wires	
M5	2000 Temp. Cycles -65°C to +200°C	1 Broken wires	12 (11) Broken wires (1) Peri-pheral open	25 Broken wires	25 Broken wires	10 Broken wires	34 Broken wires	37 Broken wires

Figure 4-2. Group 202 Failure Summary: Number Failed Out of Each Group of 50 Parts

Measurement Number	Previous Environment	TTL				CMOS		Gold Linear
		Mfr. A 7400	Mfr. B 5400	Mfr. C 5400	Mfr. D 7400	Mfr. E 4007	Mfr. C 4007	Mfr. E 741
M2	Vibration @ 20g	NO VALID FAILURES						
M3	Vibration @ 50g							
M4	Vibration @ 70g							

Figure 4-3. Group 203 Failure Summary: Number Failed Out of Each Group of 25 Parts

Measurement Number	Previous Environment	TTL				CMOS		Gold Linear
		Mfr. A 7400	Mfr. B 5400	Mfr. C 5400	Mfr. D 7400	Mfr. E 4007	Mfr. C 4007	Mfr. E 741
M2	48 hour Operating Life @ 1.09 mm Hg	NO VALID FAILURES						
M3	240 hour Operating Life @ 1.09 mm Hg							
M4	48 hour Operating Life @ $1x10^{-6}$ mm Hg							
M5	240 hour Operating Life @ $1x10^{-6}$ mm Hg							

Figure 4-4. Group 204 Failure Summary: Number Failed Out of Each Group of 50 Parts

		TTL				CMOS		Gold Linear
Measurement Number	Previous Environment	Mfr. A 7400	Mfr. B 5400	Mfr. C 5400	Mfr. D 7400	Mfr. E 4007	Mfr. F 4007	Mfr. G 741
M2	240 hours Operating Life @ +5°C	NO VALID FAILURES						
M3	760 hours Operating Life @ +5°C (1000 hours total)							
M4	240 hours Operating Life @ -55°C							
M5	760 hours Operating Life @ -55°C (1000 hours total)							

Figure 4-5. Group 205 Failure Summary: Number Failed Out of Each Group of 50 Parts

		TTL				CMOS		Gold Linear
Measurement Number	Previous Environment	Mfr. A 7400	Mfr. B 5400	Mfr. C 5400	Mfr. D 7400	Mfr. E 4007	Mfr. C 4007	Mfr. E 741
M2	1000 hour Operating Life @ 125°C				1 Plague		4 n-FET channeling	
M3	1000 hour Operating Life @ 150°C	1 Plague	1 Unexplained Short				45 n-FET channeling	6 @ 144 hrs 3 @ 168 hrs 17 @ 672 hrs Thermal Runaway 14: Thermal Degradation
M4	1000 hour Operating Life @ 175°C	39 External lead corrosion and breakage	1 Plague	1 Plague	2 Plague	10 channeling		
M5	1000 hour Operating Life @ 200°C		48 Swollen Plastic	49 Swollen Plastic	47 Swollen Plastic			

Figure 4-6. Group 206 Failure Summary: Number Failed Out of Each Group of 50 Parts

		TTL				CMOS		Gold Linear
Measurement Number	Previous Environment	Mfr. A 7400	Mfr. B 5400	Mfr. C 5400	Mfr. D 7400	Mfr. E 4007	Mfr. C 4007	Mfr. E 741
M2	1000 Temp Cycles from -55°C to +125°C							
M3	2 days Operating Life @ 1.09mm Hg (Vacuum life)							
M4	1000 hours Operating Life @ +5°C							1 Shorted MOS capacitor
M5	1000 hours Operating Life @ +125°C					4 (1) Cracked die (2) Channeling (1) Gate oxide short	4 channeling	

Figure 4-7. Group 207 Failure Summary: Number Failed Out of Each Group of 50 Parts

4.3.1 Group 201 Test Results (Continued)

The failures that resulted are shown in Figure 4-1.

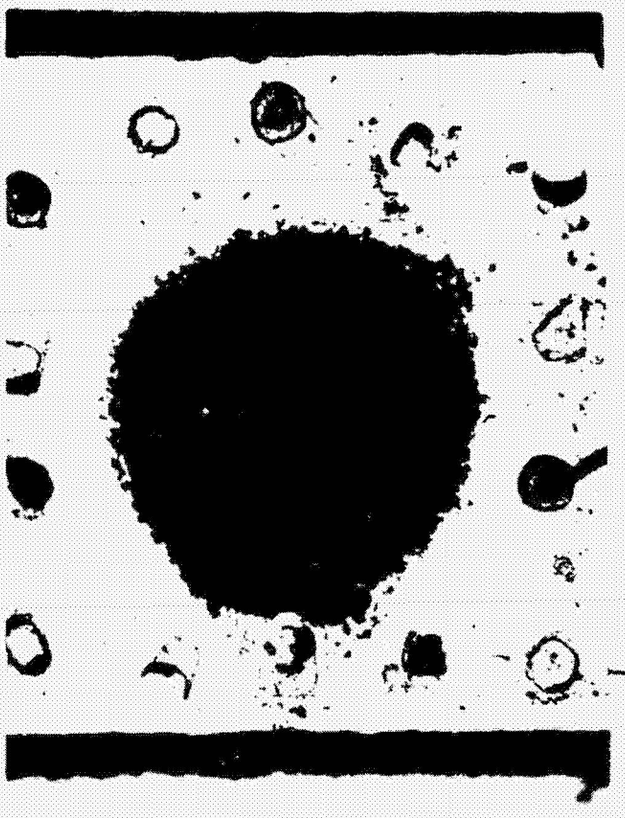
Only one TTL (bipolar) part failed in this test. The failure mechanism was a lifted or open ball bond caused by gold-aluminum intermetallic growth (plague). See Figure 4-8. However the prior environments of thermal shock and moisture resistance are not thought to be the cause. Instead this is felt to be a freak failure, a part which failed for causes totally unrelated to the environment. Plague failures generally occur as a result of exposure to high temperature for extended periods of time. The total high temperature exposure of this part was not enough to cause plague in a well made part. However in a given lot of commercial grade high volume parts, a certain population of poorly made parts can be expected, and this failure can be attributed to such a freak population occurrence.

For the CMOS parts, two predominant failure causes were noted. After the moisture resistance environment, three Mfr. E and one Mfr. C parts were found to have failed. These parts were retested to verify the failures, and then were baked for 96 hours at first 150°C and then 175°C. Two of the three Mfr. A parts recovered after 96 hours at 150°C, and the third recovered after 96 additional hours at 175°C. The conclusion drawn is that water absorbed by the encapsulant and intruding onto the chip surface caused sufficient leakage current to disrupt circuit operation, and that bakeout removed the water and restored proper operation. For the one Mfr. C part, no recovery was observed even after 96 hours bake at 175°C, so the part was dissected. The results showed massive circuit disruption: open circuits caused by apparent electrical abuse (See Figure 4-9). Since the part had not been subjected to any operating life test, the abusive currents could have only been provided during electrical measurement. The tester currents are normally self limited to non-destructive levels, hence it is postulated that absorption of moisture by the device permitted excessive currents to flow during testing performed prior to bake out.

The other predominant CMOS failure mechanism observed was channeling of the n-channel FETS after the final environmental stress of 1000 hour operating life at 125°C. Six Mfr. E and 24 Mfr. C parts showed this failure mechanism, which was found to be a common one for CMOS under elevated temperature operating life.

Channeling failures occurred in 3 areas of the CMOS devices: 1) input gate protection diodes, 2) p-channel FETS, and 3) n-channel FETS. Figure 4-10 shows the recovery of a channeled input gate protection diode network as a result of baking the part at 150°C for various periods of time: 15 hours, 30 hours and 100 hours. Figure 4-11 shows the partial recovery of an n-channel FET after bake at 150°C for 30 hours. Figure 4-12 shows the recovery of a p-channel FET after bake at 150°C for 30 hours. This series of pictures (Figures 4-10, -11, -12) were all recorded on a single part, Mfr. E serial number 2103.

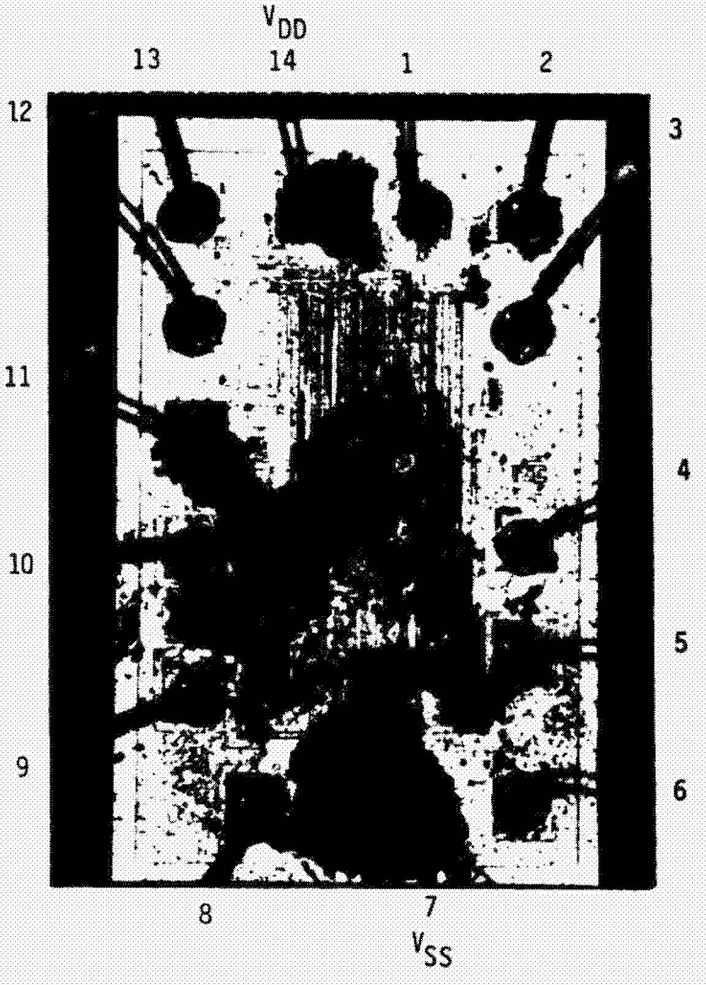
A more complete example of n-channel recovery is shown in Figure 4-13, which shows the improvement in drain to source leakage current after first 100 hours and then 300 hours bake at 150°C.



Magnification = 80X

TTL 7400
Manufacturer D,
Serial Number 1605
Prior Environmental Stress: 15 Thermal Shock Cycles, -65°C to +150°C
10 day Moisture Resistance
Cause of Failure: Gold-Aluminum intermetallics (plague) under ball bonds.
Bonds lifted after encapsulant was stripped.

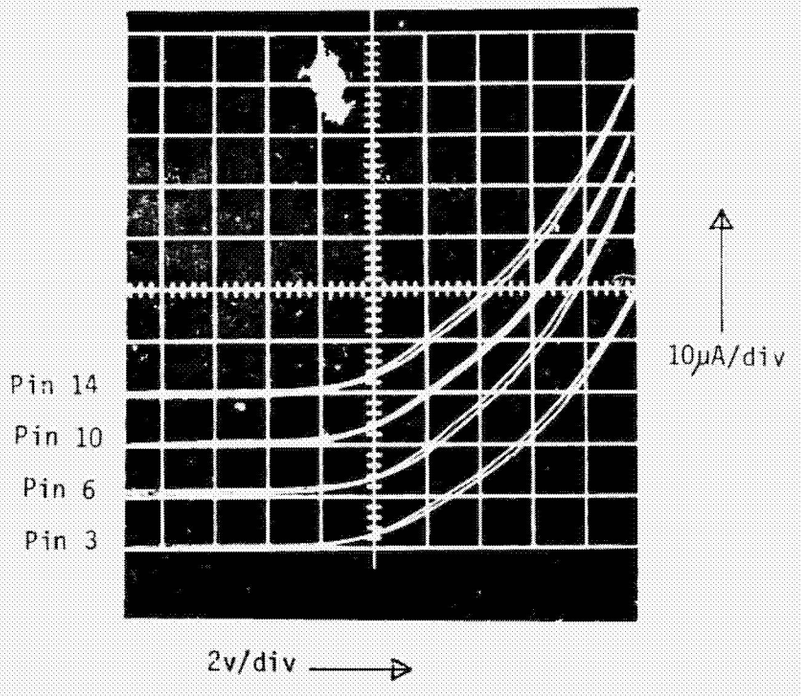
Figure 4-8 Group 201 TTL Mfr. D Failure: Plague



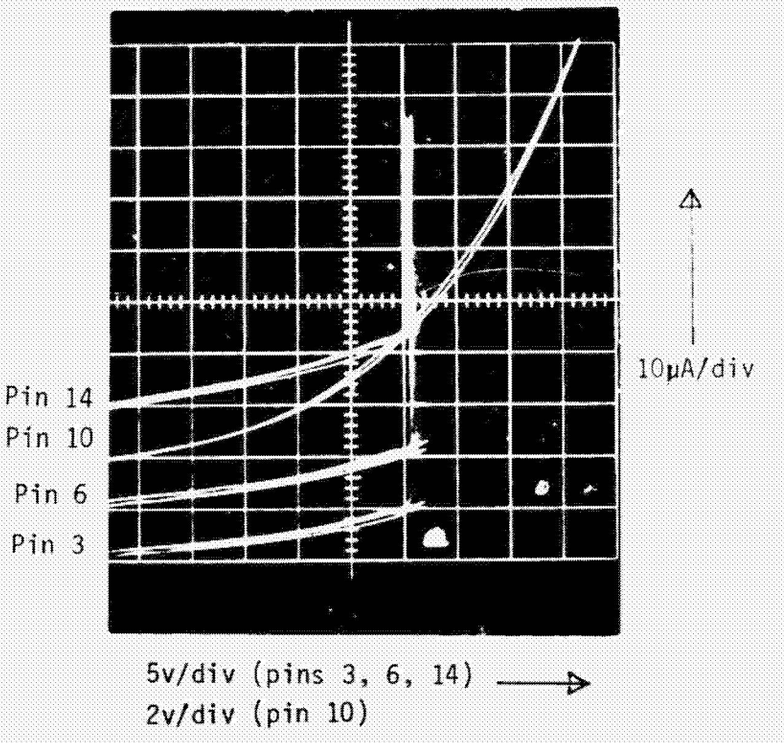
Magnification = 80X

CMOS 4007
Manufacturer C
Serial Number 2620
Prior Environmental Stress: 15 Thermal Shock Cycles, -65°C to +150°C
10 day Moisture Resistance
Cause of Failure: Excessive electrical current during electrical testing, due to moisture absorption.

Figure 4-9. Group 201 CMOS Mfr. C Failure: Moisture Absorption



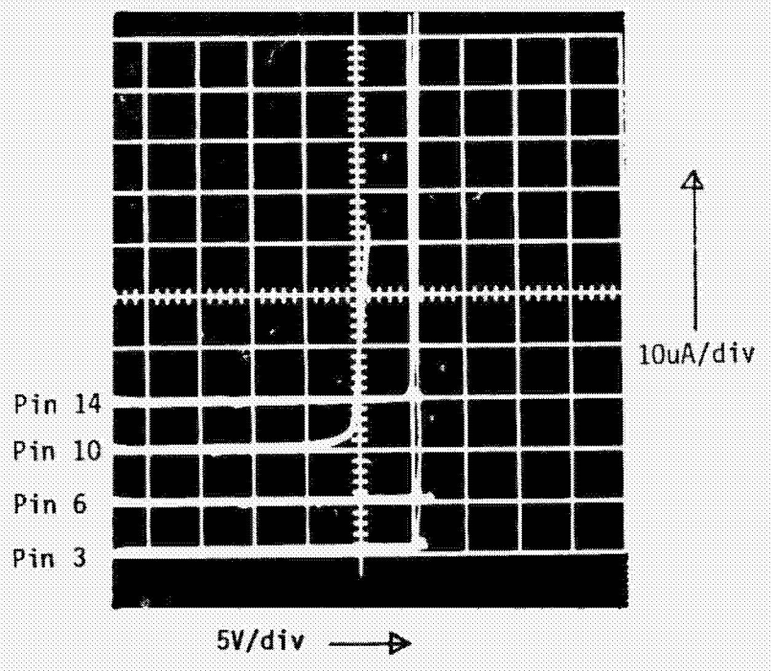
a) I-V characteristic measured from indicated pin to pin 7 (GRD) before any bake out, after failure was found electrically.
Shows channeling of gate protection diodes.



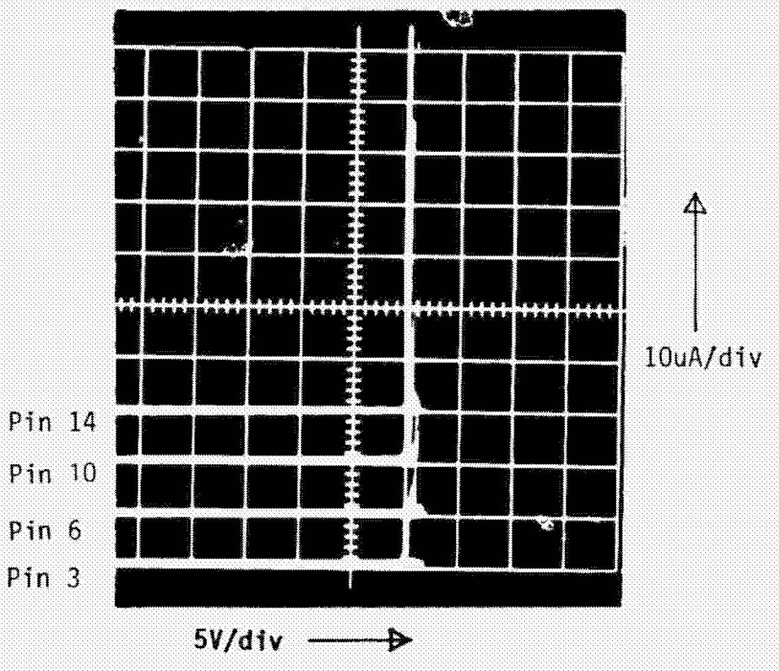
b) 15 hour bake out at 150°C.
I-V characteristic from indicated pin to pin 7 (GRD)
Shows partial recovery of channeled structures.

CMOS 4007 Serial Number 2103
Manufacturer E Prior Environmental Stress: 15 Temperature Cycles -65 to +150°C, 10 day humidity, 1000 hour operating life at +5°C, 1000 hour operating life at +125°C.

Figure 4-10. Group 201 CMOS Mfr. E Failure: Channeling of Gate Protection Diodes

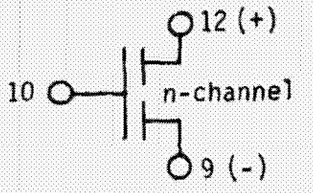


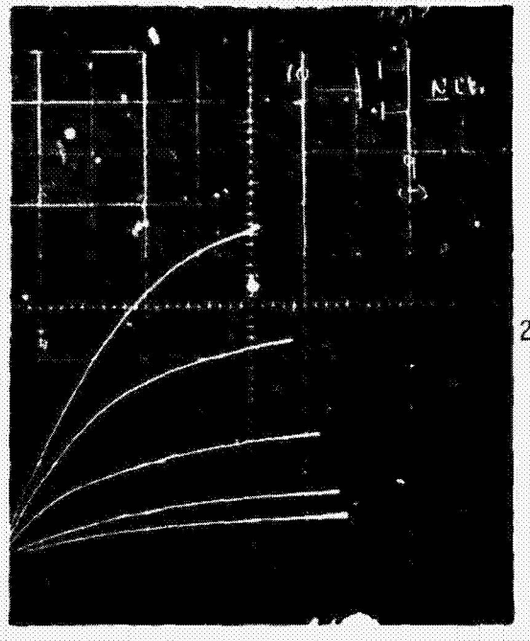
c) 30 hour bake out at 150°C.
I-V characteristic from indicated pins to pin 7 (GRD).
Shows nearly complete recovery of channeled structures.



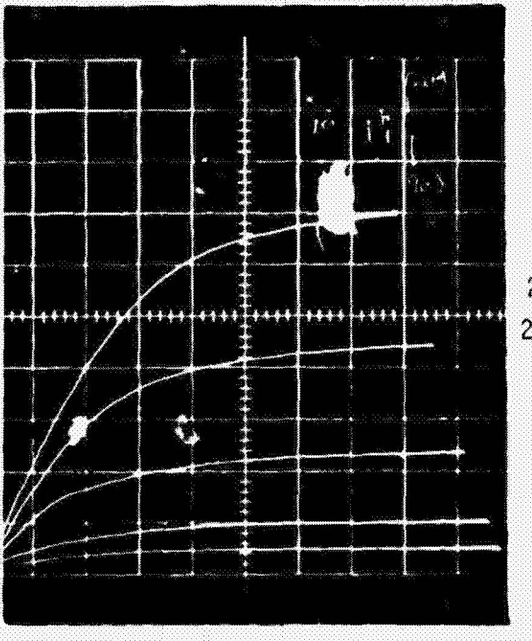
d) 100 hour bake out at 150°C.
I-V characteristic from indicated pins to pin 7 (GRD)
Shows complete recovery of channeled structures.

Figure 4-10 (continued). Group 201 CMOS Mfr. E Failure: Channeling of Gate Protection Diodes





a) Before bake out, but after electrical failure. n-channel transistor curves.

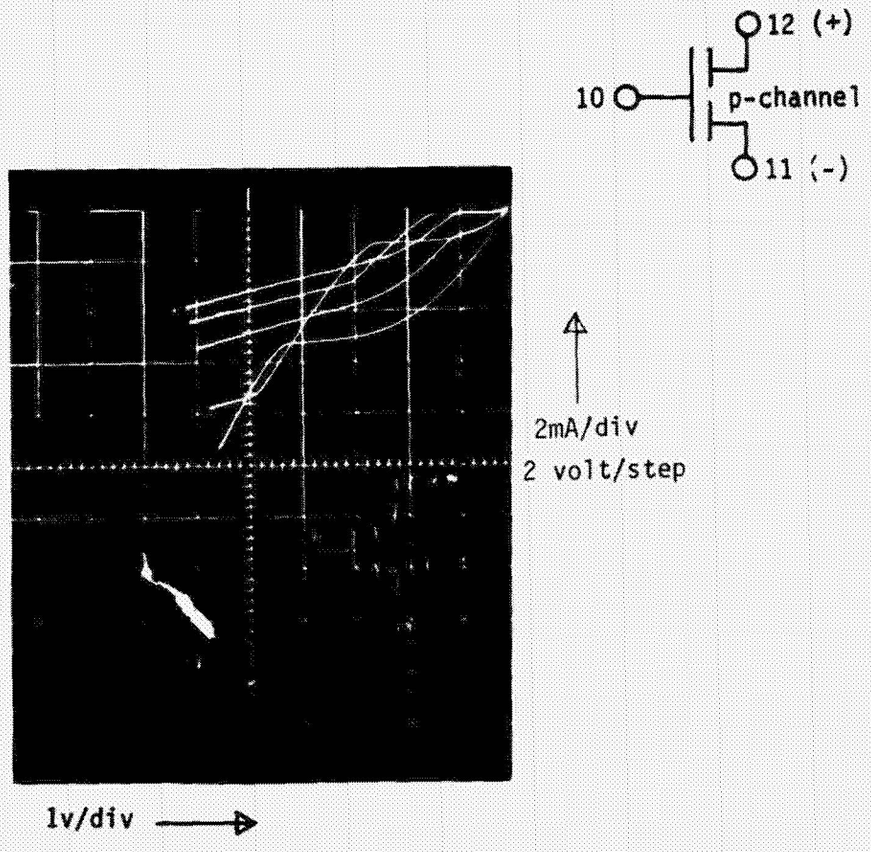


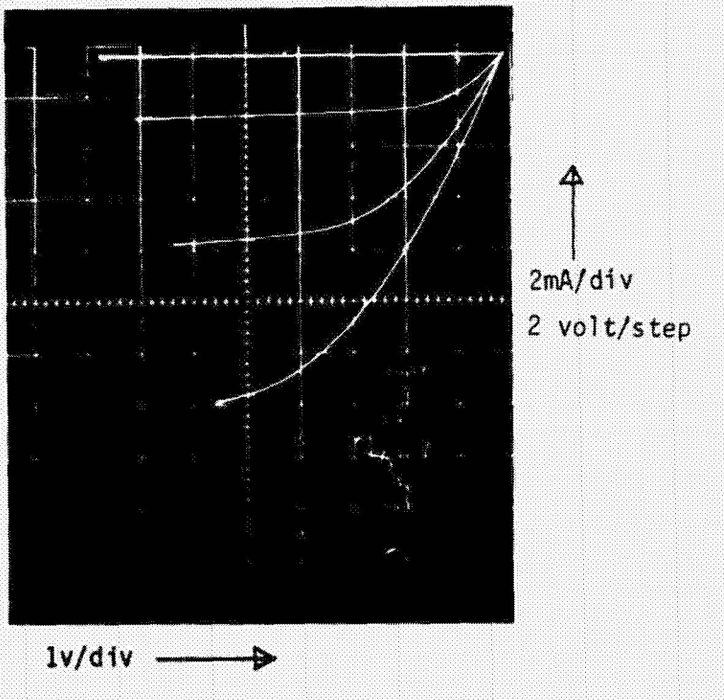
b) After 30 hour bake at 150°C. Note improved source/ Drain Leakage (0v input step)

CMOS 4007 Serial Number 2103
Manufacturer E P. or Environmental Stress: Thermal Shock, 10 day Humidity, 1000 hour operating life at 5°C, 125°C.

Figure 4-11 Group 201 CMOS Mfr. E Failure: Channeling of n-FET

D180-20546-1





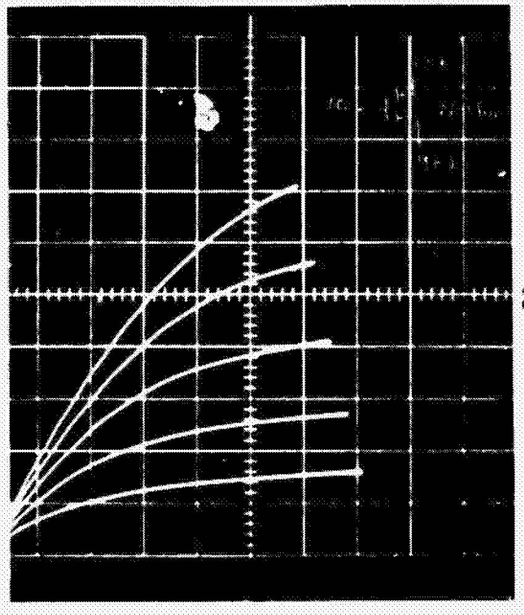
a) Before bake but after electrical failure. P-channel transistor curves.

b) After 30 hour bake at 150°C. Behavior now normal.

CMOS 4007 Serial Number 2103
Mfr. E Prior Environment: Thermal Shock, 10 day Humidity, 1000 hour operating life @ 5°C, 125°C.

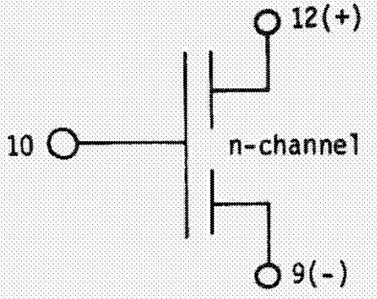
Figure 4-12. Group 201 CMOS Mfr. E Failure: Channeling of p-FET

D180-20546-1



1v/div

2mA/div
2 volt/step



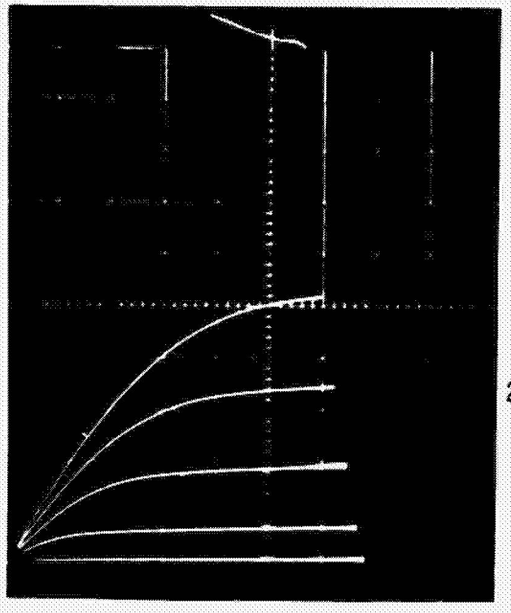
a) Before bake out but after electrical failure. Drain/Source Leakage = 2.8mA @ 5v V_{DS}

D180-20546-1

CMOS 4007
Mfr. C

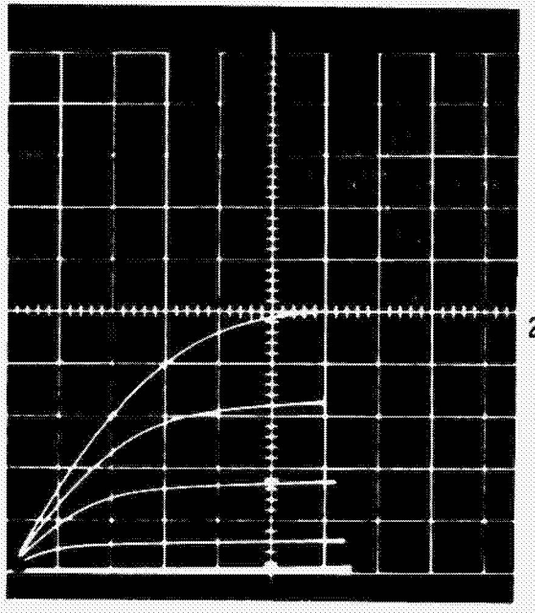
Serial Number 2607
Previous Environment: Thermal Shock, 10 day Humidity, 1000 operating life @ 5°C, 125°C

Figure 4-13 Group 201 CMOS Mfr. C Failure: n-FET Channeling



b) After 100 hour bake at 150°C. Drain/Source Leakage = 160μA @ 5v V_{DS}

CMOS 4007 Serial Number 2607
Manufacturer C



c) After 300 hour bake at 150°C. Drain/Source Leakage = 16μA @ 5v V_{DS}

Figure 4-13 (continued). Group 201 CMOS Mfr. C Failure: n-FET Channeling

4.3.2 Group 202 Test Results

This group received the following environmental stresses:

1000 Temperature Cycles from -55°C to +. °C
M2
1000 Temperature Cycles from -55°C to +125°C
M3
2000 Temperature Cycles from -65°C to +150°C
M4
2000 Temperature Cycles from -65°C to +200°C
M5

The predominant failure mechanism in this test group, as might be expected, was broken lead wires as shown in Figures 4-14 and 4-15. The significant thing about the failures that occurred is the distribution of failures versus number of cycles for each vendor.

The parts experienced 10 minutes at each temperature each cycle, so 2000 cycles exposed the parts 20,000 minutes at +200°C. This is 333 hours, not as severe as the 1000 hours of operating life experienced by Group 206, but approaching the region where the swelling plastic might have begun to occur (see 4.3.6). Yet only one of the Mfr. A TTL parts failed at this extreme, while large numbers of other manufacturers parts failed here.

For Mfr. B, no failures occurred until the final increment when 11 broken wire failures occurred and one additional part failed due to an open bond. This bond failure (pin 1) was diagnosed as a peripheral open. When the part was dissected it was found that the bond was still firmly attached to the underlying metal. See Figure 4-16. However electrical probing of the bond and the metallization showed that there was an open circuit between the ball of the bond and the aluminum metallization. This indicates that the periphery of the ball bond had degraded enough to cause the open circuit but the main contact area of the bond was still intact.

For Mfr. C (TTL), one failure occurred after 2000 cycles from -55°C to +125°C, three more occurred after 2000 cycles from -65°C to +150°C and twenty-five failures occurred in the final increment, 2000 cycles from -65°C to +200°C, for a total of 29 failures. For Mfr. C (CMOS) the performance was even worse. Nine failures occurred after the third test increment of 2000 cycles from -65°C to +150°C and thirty-four additional failures occurred in the final increment for a total of 43 failures.

For Mfr. D, twenty-five parts failed in the final test increment, but none occurred previously.

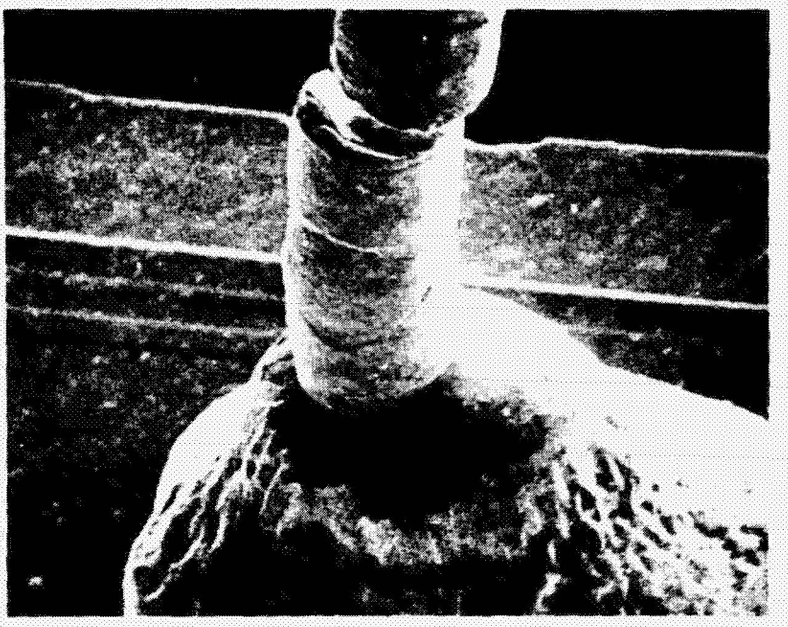
For Mfr. E (CMOS), only ten broken wire failures occurred and off of these were after the last stress increment.

Many of the failures due to broken wires were only observed during the +125°C electrical measurement, indicating that at -55°C and +25°C the broken wire ends were making adequate enough contact to avoid detection. Since "hot intermittent opens" (HIO) failures were commonly observed with pre-novolac encapsulated microcircuits, the occurrence of these failures at +125°C only is of concern. Figure 4-17 shows the number of "+125°C only" (or HIO) failures that occurred.

800X

(a) Mfr. B, Serial Number 659. TTL 5400
Previous Environmental Stress: 2000 cycles each at -55°C to +125°C
-65°C to +150°C
-65°C to +200°C

Figure 4-14. Group 202 Representative TTL, CMOS and Linear Broken Wire Failures



800X

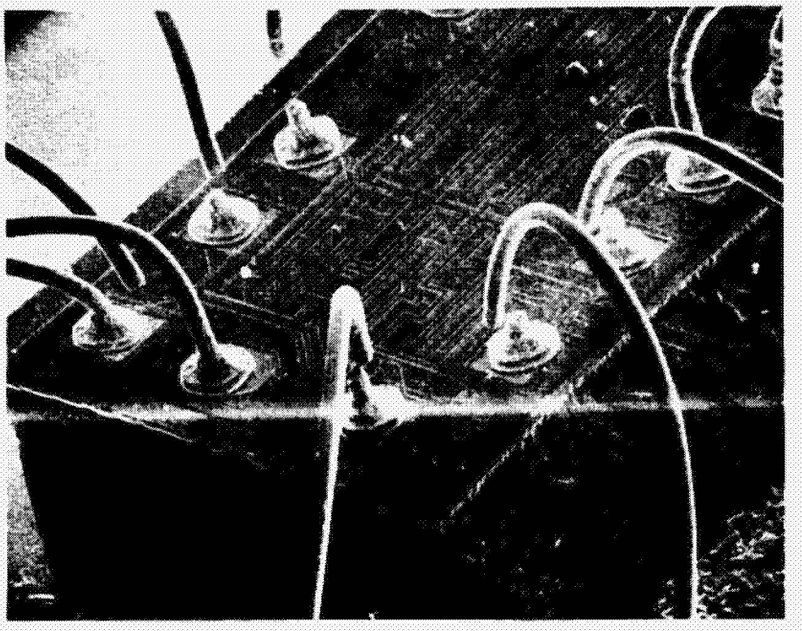
(b) Mfr. D, Serial Number 1682, TTL 5400

Figure 4-14 (continued). Group 202 Representative TTL, CMOS and Linear Broken Wire Failures

800X

(c) Mfr. E, Serial Number 2232, CMOS 4007

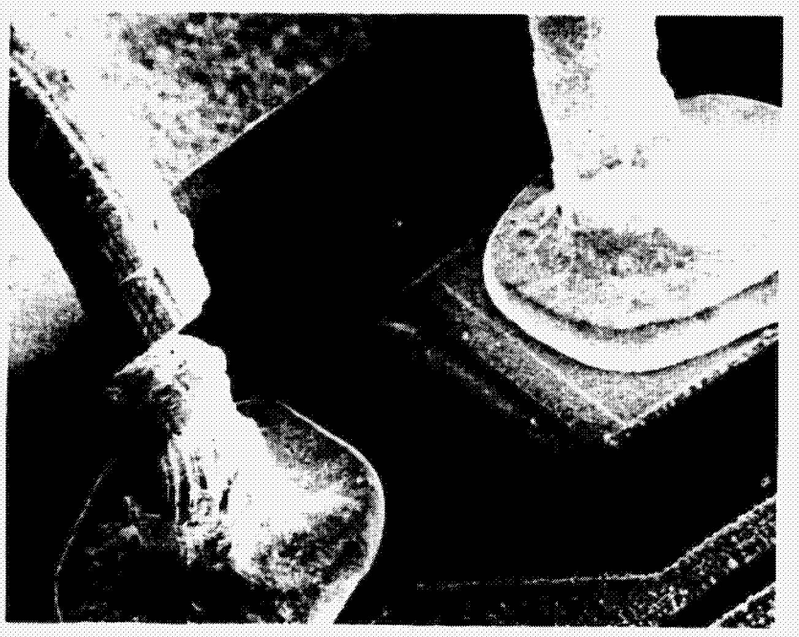
Figure 4-14 (continued). Group 202 Representative TTL CMOS Broken Wire Failures



100X

(d) Mfr. C, Serial Number 2683, CMOS 4007

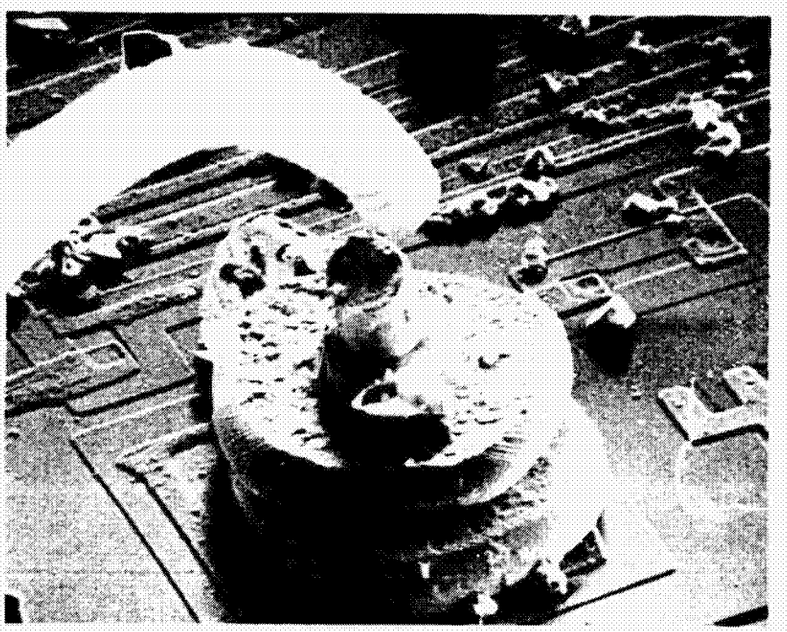
Figure 4-14 (continued). Group 202 Representative TTL, CMOS and Linear Broken Wire Failures



400X

(e) Mfr. C, Serial Number 3532, Gold Metallized Linear 741

Figure 4-14 (continued). Group 202 Representative TTL, CMOS and Linear Broken Wire Failures

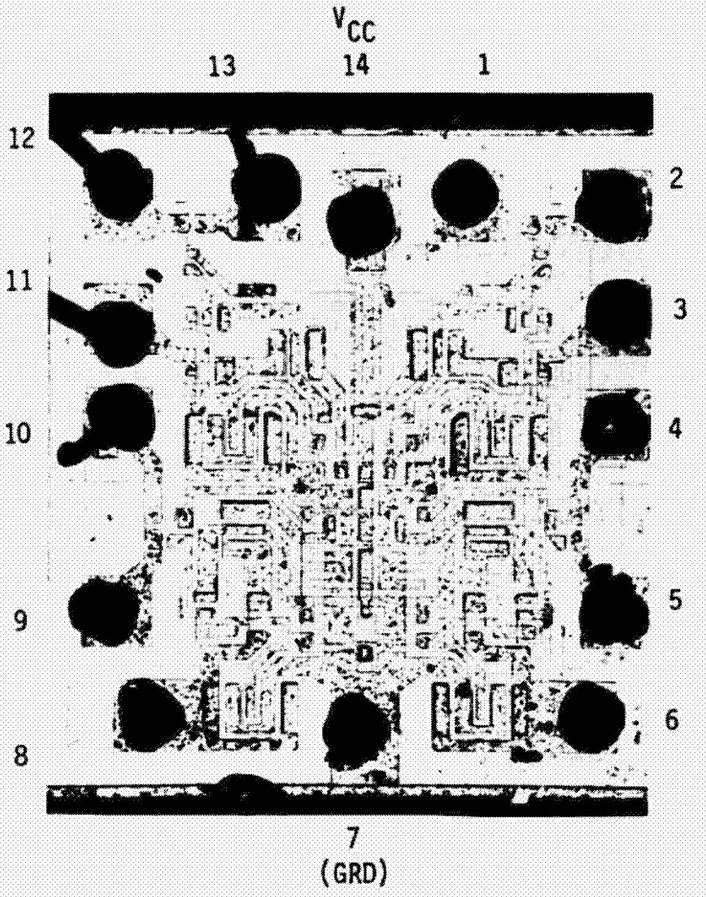


400X

Note the double bond. Failure still occurred above the bond.

CMOS 4007
Manufacturer C
Serial Number 2724
Cause of Failures: Broken lead wires
Previsou Environmental Stress: 2000 Temperature cycles at -55°C to +125°C
-65°C to +150°C.

Figure 4-15. Group 202 CMOS 4007 Mfr. C Failure: Broken Wires



TTL 5400
Manufacturer B
Serial Number 665
Cause of Failure: Peripheral open on Pin 1
Previous Environmental Stress: 2000 Temperature cycles from -55°C to +125°C
2000 Temperature cycles from -65°C to +150°C
2000 Temperature cycles from -65°C to +200°C.

Figure 4-16. Group 202 TTL Mfr. B Failure: Peripheral Open

Measurement Number	Previous Environments	Mfr.	Part Type	Total Broken Wire Failures	"+125°C Only" Failures
M3	2000 Temp Cycles -55°C to +125°C	C	TTL 5400	1	1
M4	2000 Temp Cycles -65°C to +150°C	C C	TTL 5400 CMOS 4007	3 9	0 0
M5	2000 Temp Cycles -65°C to +200°C	A B C D E C E	TTL 7400 TTL 5400 TTL 5400 TTL 7400 CMOS 4007 CMOS 4007 Linear 741	1 11 25 25 10 34 37	0 4 0 1 8 3 8
			Total	156	25

Figure 4-17. Summary of "+125°C Only" Failures Due to Broken Wires After Thermal Cycling

4.3.2 Group 202 Test Results (Continued)

Only one HIO failure occurred before the final extremely severe thermal cycling stress. As a result the possible incidence of hot intermittent opens can be considered negligible in modern novolac encapsulated microcircuits, particularly in view of the fact that in pre-novolac encapsulated microcircuits the HIO failures generally resulted from the elevated temperature causing bond wires to lift off the bonding pads during measurement.

Two freak failures occurred after the second increment (total of 2000 cycles from -55°C to +125°C). One of these resulted from a cracked die (Figure 4-18) and the other from an open ball bond which showed the symptoms of being a "peripheral" open; that is, a ball bond which failed around the periphery of the gold-to-aluminum interface rather than under the heart of the ball bond.

The Mfr. E linear parts, which employ gold lead wires rather than aluminum, experienced no failures until the last increment when thirty-seven parts failed due to broken wires. This again could have been caused by thermal cycling stress or by deformation or swelling of the epoxy encapsulant as a result of 333 hours of exposure to 200°C, although no visible evidence of swelling was observed.

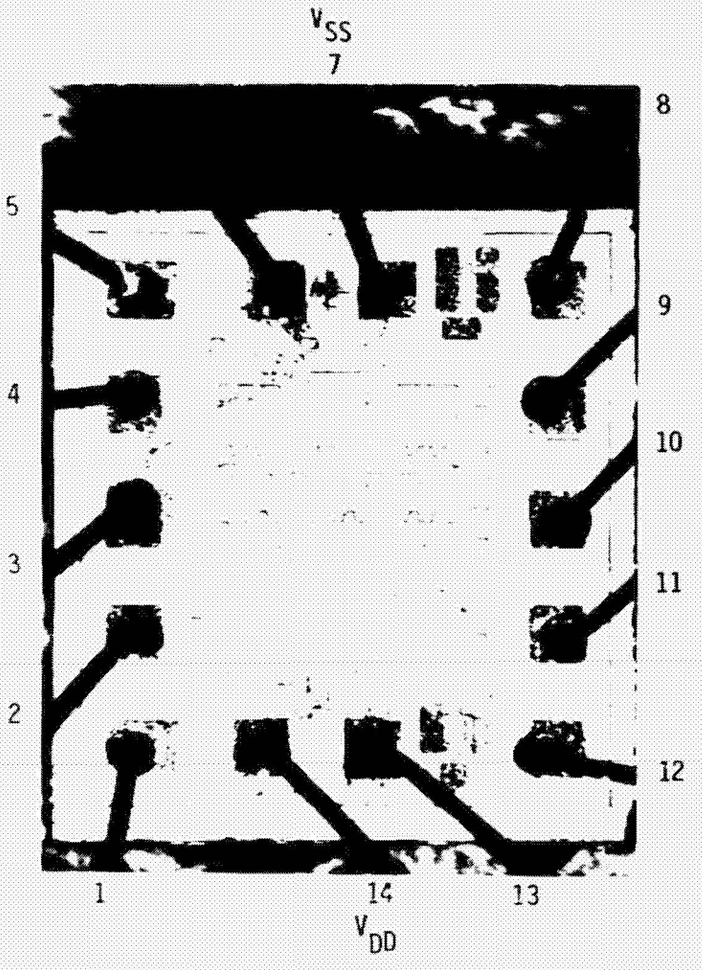
4.3.3 Group 206 Test Results

This group received the following environmental stresses

1000 hour operating life at 125°C
M2
1000 hour operating life at 150°C
M3
1000 hour operating life at 175°C
M4
1000 hour operating life at 200°C
M5

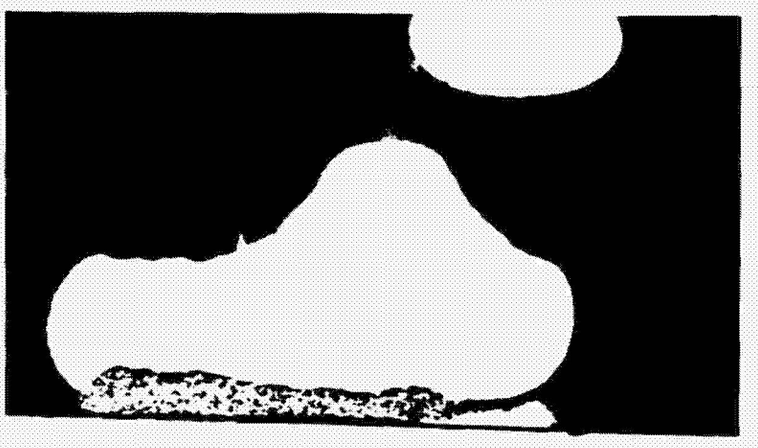
For the TTL parts three primary failure mechanisms of interest occurred. These are gold-aluminum bond plague external lead corrosion, and deformation of encapsulant. One plague failure was observed in Mfr. D TTL parts after 125°C 1000 hour operating life, and then after 175°C 1000 hour operating life, Mfr. D had two more plague failures, Mfr. C had one, and Vendor B had one. Mfr. B TTL parts also experienced one freak failure due to a diffusion short after 150°C operating life.

These plague failures were all of a different nature than is normally encountered in gold-aluminum bond systems. Ordinarily when Kirkendall diffusion occurs in gold-aluminum bonds, the ball separates cleanly from the underlying aluminum metallization. However as seen in Figure 4-19, it appears that the epoxy encapsulant held the bonds tightly in place and prevented them from separating from the substrate. Kirkendall diffusion then proceeded, forming a large region of intermetallic growth between the gold region and the aluminum region which finally developed enough voids to cause an open circuit.



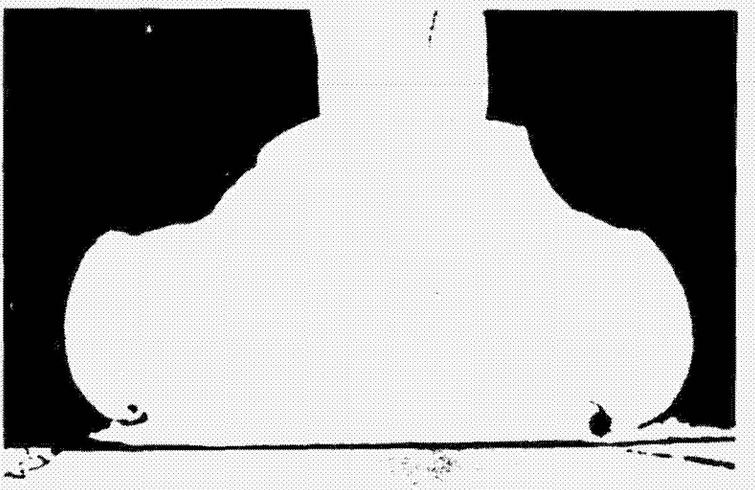
CMOS 4007
Manufacturer E
Serial Number 2230
Cause of Failure: Cracked die causing pins 6 and 13 to short to pin 7.
Previous Environmental Stress: 2000 Temperature cycles from -55°C to +125°C.

Figure 4-18. Group 202 CMOS Mfr. E Failure: Cracked Die



800X

(a) Plastic Plague after 1000 hours Operating Life at 125°C, 150°C, 175°C.



800X

(b) Normal Bond after 1000 hours Operating Life at 125°C, 150°C, 175°C.

Figure 4-19. Plastic Plague Compared to Normal Gold-Aluminum Intermetallic

4.3.3 Group 206 Test Results (Continued)

Figure 4-20 shows a top view of a typical plastic plague failure, while Figure 4-21 shows views of the interface between the bond and the aluminum metallization. Note the extremely rough, porous-appearing material at the interface. Figures 4-22 and -23 show additional examples of plastic plague.

This phenomenon of "plastic plague" has not been observed previously and represents a new failure mechanism present with epoxy encapsulated microcircuits. However this mechanism only appeared in force after quite extensive stress testing and does not appear to represent a threat to device integrity at normal usage levels.

The second predominant TTL failure mechanism occurred in Manufacturer A parts after 175°C operating life. Thirty-nine out of the 49 parts tested failed due to broken external leads: all 49 devices had leads which had become very brittle and which in addition had badly corroded plating resulting in a mottled brown discoloration. Sample electrical testing on seven out of the 39 failed parts showed that the internal circuitry was still functioning, but accurate automatic electrical tests and subsequent high temperature operating life tests could not be made because of the broken external leads. See Figure 4-24.

Metallurgical analysis of the cause of the failures resulted in the determination that the silver plated Alloy 42 leads had suffered: severe stress corrosion cracking caused by chloride ions attacking the Alloy 42.

Microprobe analysis of a fractured surface of a lead showed the following concentration of elements:

Strong	Weak	Very Weak
Fe, Ni	Co, Mn, Cr, Cl	Si, Cu

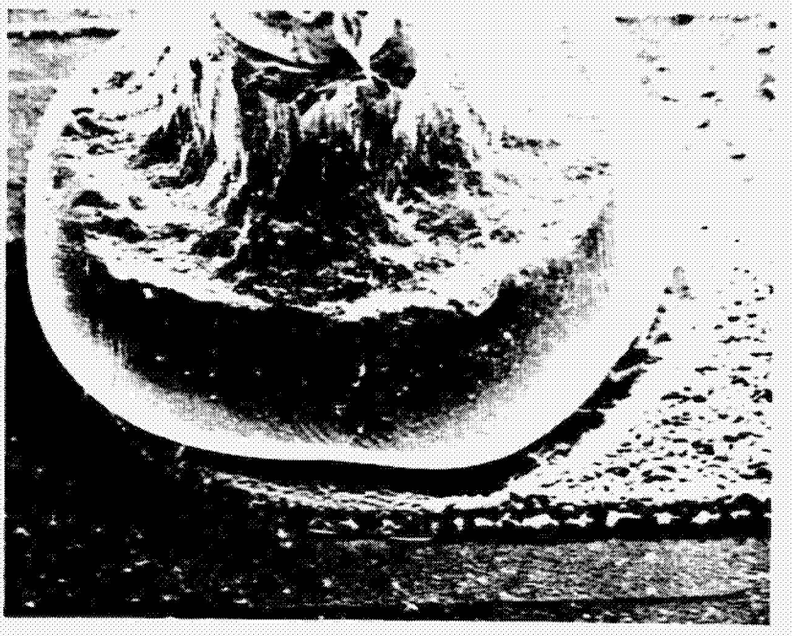
The plating was confirmed as being silver with no detectable contaminants.

The gold-brown discoloration/contamination was also analyzed. This showed the following relative concentration of elements:

Strong	Medium Weak	Weak
Fe, Ni	Cl	Cu, Co, Mn, Cr, Si

Photomicrographs of specimen leads showed considerable internal cracking as shown in Figures 4-25 and 4-26. Photo-micrographs of etched specimens (Figures 4-27, 4-28) show that the cracking is quite severe. In all cases, the cracking appeared to be less severe when the silver plating was tightly adherent.

Manufacturer A parts were examined which had not received the high temperature environmental stress but had received the initial Class B screening including 160 hours at 125°C. The photomicrographs of these parts showed that in some cases some darkening of the silver plate had occurred on one side of the lead as shown in Figure 4-29. A high magnification photomicrograph of this darkened section is shown in Figure 4-30, where a surface reaction product can also be seen.



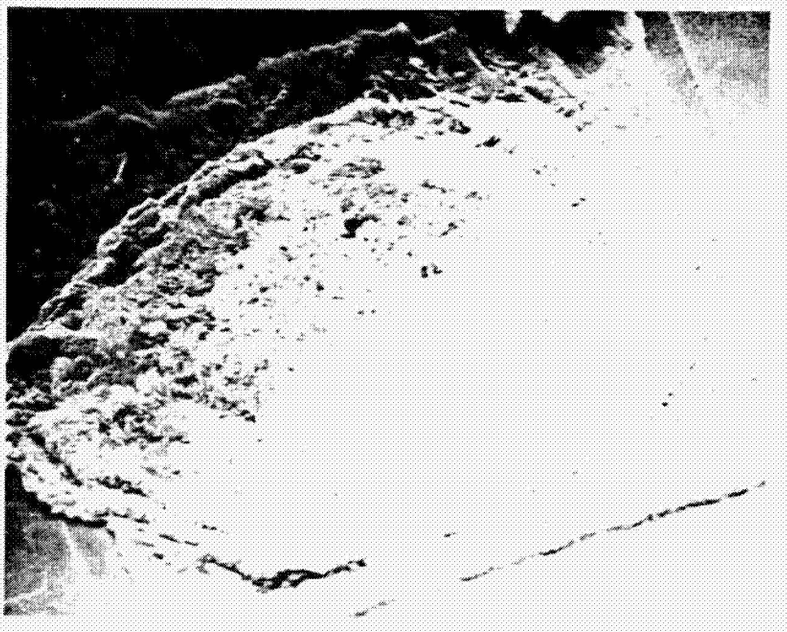
700X

(a) Bond and pad

TTL 7400
Manufacturer D
Cause of Failure: Gold-aluminum intermetallic growth
Previous Environmental Stress: 1000 hour Operating Life @ 125°C

Figure 4-20. Group 206 TTL Mfr. D Failure: Gold-Aluminum Bond Degradation - Plastic Plague

(a) Underside of gold ball 1000X



(b) Aluminum bond g pad 1000X

Figure 4-21. Group 206 TTL Mfr. D Failure: Gold-Aluminum Bond Degradation - Plastic Plague

700X

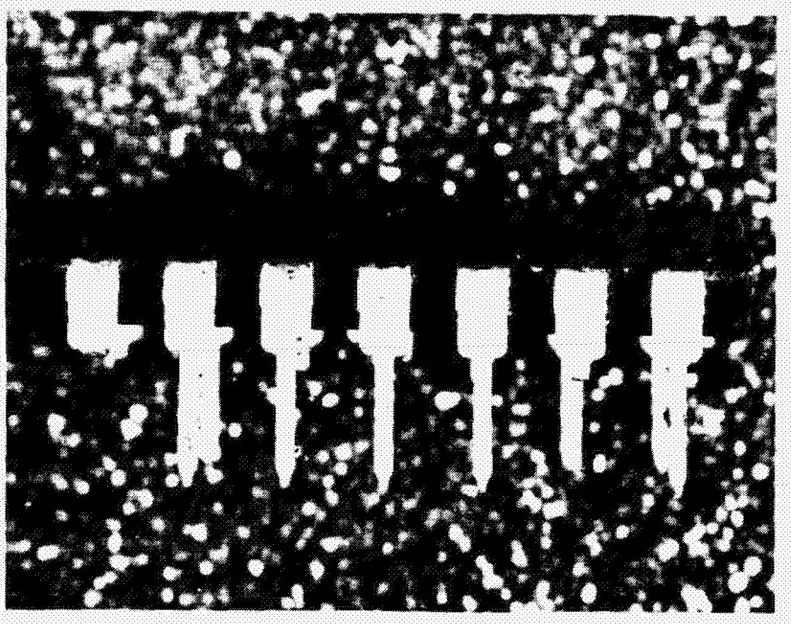
TTL 5400
Manufacturer B
Serial Number 891
Cause of Failure: Open circuit due to Gold-Aluminum intermetallic growth under ball bond
Previous Environmental Stress: 1000 operating life at 125°C
150°C
175°C.

Figure 4-22 Group 206 TTL Mfr. B Failure: Plastic Plague

1326X

TTL 5400
Manufacturer C
Serial Number 1417
Cause of Failure: Open Circuit due to Gold-Aluminum intermetallic growth under ball bond
Previous Environmental Stress: 1000 hour Operating Life at 125°C
150°C
175°C.

Figure 4-23. Group 206 TTL Mfr. C Failure: Plastic Plague



TTL 7400
Manufacturer A
Serial Number 382 (example of 39 total failures)
Cause of Failure: Severe corrosion and embrittlement of external leads, causing breakage of multiple pins
Previous Environmental Stress: 1000 hour Operating Life at: 125°C
150°C
175°C

Figure 4-24. Group 206 TTL Mfr. A Failure: Lead Corrosion

250X

Figure 4-25. Photomicrograph of Fractured Lead

250X

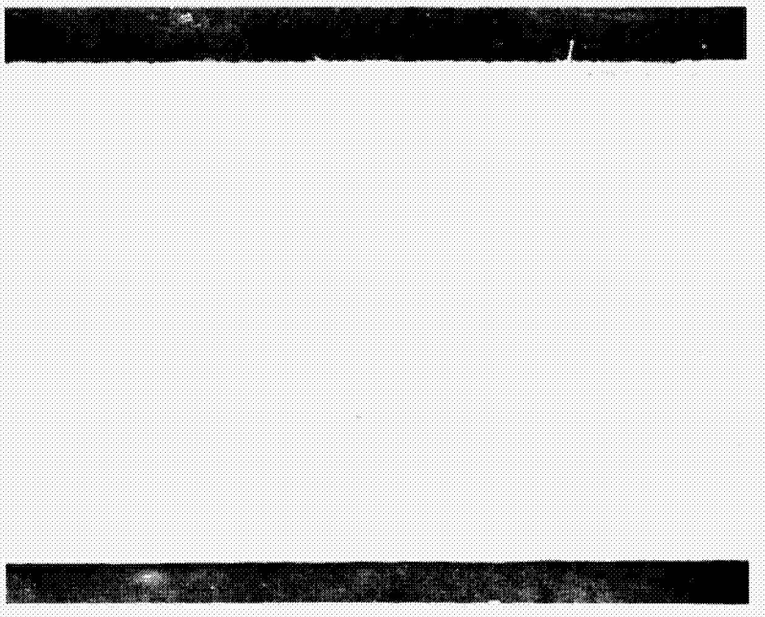
Figure 4-26. Photomicrograph of Cracking Lead

250X

Figure 4-27. Photomicrograph of Etched Lead

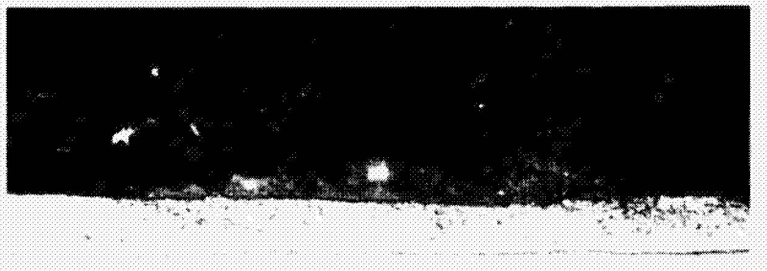
250X

Figure 4-28. Photomicrograph of Etched Lead at Bend



250X

Figure 4-29. Lead Cross Section Before High Temperature Stress.



1000X

Figure 4-30. Close-up of Surface Reaction Production

4.3.3 Group 206 Test Results (Continued)

There are two possibilities for the contact of the device-lead alloy with chloride-ion solutions. One of these is that inadequate removal of a chloride oxide stripper was done prior to silver plating. It is even possible that the leads were not completely stripped of oxide and mixed oxide-chloride patches were retained on the surface going into the plating bath.

The second possibility is that the plated leads were exposed to a chloride environment. The damage then ensued as a result of chloride ion penetration into localized damage spots in the silver surface.

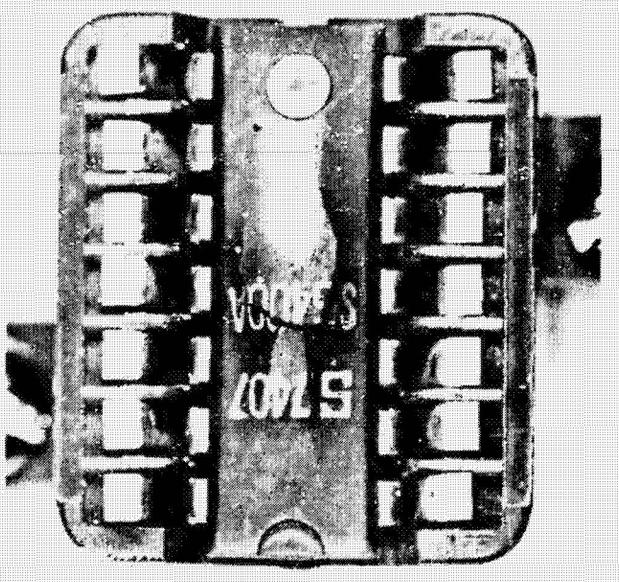
In either instance, there were two corrosion reactions experienced by the leads. The first of these was a general corrosion reaction resulting in surface damage and the development of voluminous corrosion products. The second and more damaging reaction was stress corrosion cracking which resulted in deep transgranular cracking and the consequent weakening of the sections.

The stress corrosion cracking was not limited to the bent regions of the leads but was seen also in the straight sections. This means that the leads were in a condition of residual tensile stress as installed in the D.I.P. unit. This factor contributed to the stress corrosion reaction.

The final failure mechanism observed in the TTL parts occurred in the three devices types (Manufacturers B, C, and D) which still survived after M4 and were put into operating life test for 1000 hours at 200°C. All 150 parts in these three cells experienced massive swelling and deformation of the epoxy encapsulant (see Figure 4-31) which resulted in broken lead wires and universal failure. The "glass transition temperature" (that is the temperature at which the encapsulants co-efficient of thermal expansion changes markedly) is claimed to be around 175°C, thus the exposure to 200°C temperature alone should have caused some circuit disruption. However the parts were all monitored at the start of the 1000 hour operating life test at 200°C, and were operating normally. Apparently, prolonged exposure to the 200°C environment caused severe degradation of the encapsulants, and caused it to expand by 10 to 25%. This expansion manifested itself as swelling: each part appeared to have swollen and cracked down the middle.

One freak failure occurred after the 150°C increment of 1000 hour operating life. A Manufacturer B TTL 5400 part was found to have a short circuit from pin 8 (output 3Y) to pin 7 (ground). This particular part type did not employ a glassivated surface, and when the encapsulant was stripped, all the aluminum metallization also came off. As a result the cause of the short circuit could not be determined by either probing, visual microscopic examination, or SEM examination.

The CMOS part types (Manufacturers E and C) exhibited only one basic failure mechanism under conditions of high temperature operating life: channeling. The channeling failures were verified by subjecting samples out of the failed parts to non-biased bake out at elevated temperatures and looking for reheal. These parts universally were restored to initial operating conditions by applying a bake stress roughly equivalent to the initial high temperature operating life stress.



TTL 7400/5400
Manufacturer B (also C and D)
Cause of Failure: Expansion of the epoxy encapsulant breaking internal lead wires.
Previous Environmental Stress: 1000 hour Operating Life at: 125°C
150°C
175°C
200°C.

Figure 4-31 Group 206 TTL Typical Swollen Encapsulant Failure
(Manufacturers B, C, and D)

4.3.3 Group 206 Test Results (Continued)

The Mfr. C parts showed four channeling failures after 1000 hours operating life at 125°C and 45 channeling failures after 1000 hours operating life at 150°C, at which time the test was terminated.

The Mfr. E parts showed ten catastrophic channeling failures after 1000 hours operating life at 175°C, but there were so many marginal parts showing symptoms of input diode channeling that the test was terminated at this point.

An attempt was made to determine if the epoxy encapsulant was responsible for the channeling. This was not an easy task for autopsy. The sensitivity of the electrical phenomena of the CMOS devices to contaminants exceeds the detection limits of any applicable analytical tool. The one possibility that was briefly examined was the possibility that charge separation or the formation of "electrets" might be causing the channeling. One CMOS unit which had channeled and had been repaired by high temperature storage was returned to burn in until it re-channeled. The encapsulant was then chemically removed and the device retested. It was still channeled, suggesting at least that electrets in the encapsulant was not the cause of the channeling phenomena.

The linear microcircuits experienced a still different failure mechanism during the 1000 hour operating life test at 150°C. The circuits were biased according to the MIL-specification bias circuit. After 144 hours, six of the devices went into thermal runaway, overheated, and caught fire. At 168 hours three more parts overheated and charred, and at 672 hours seventeen additional parts overheated and charred. The test was terminated at this time. Electrical tests performed on the survivors showed that fourteen additional parts had suffered thermal degradation sufficient to cause electrically abusive currents to flow. Figure 2-8 shows the percent failed versus the log of time. Figure 4-32 shows a typical part which failed due to thermal runaway. The white rectangle is comprised of the ash left after the combustible products in the encapsulant were consumed.

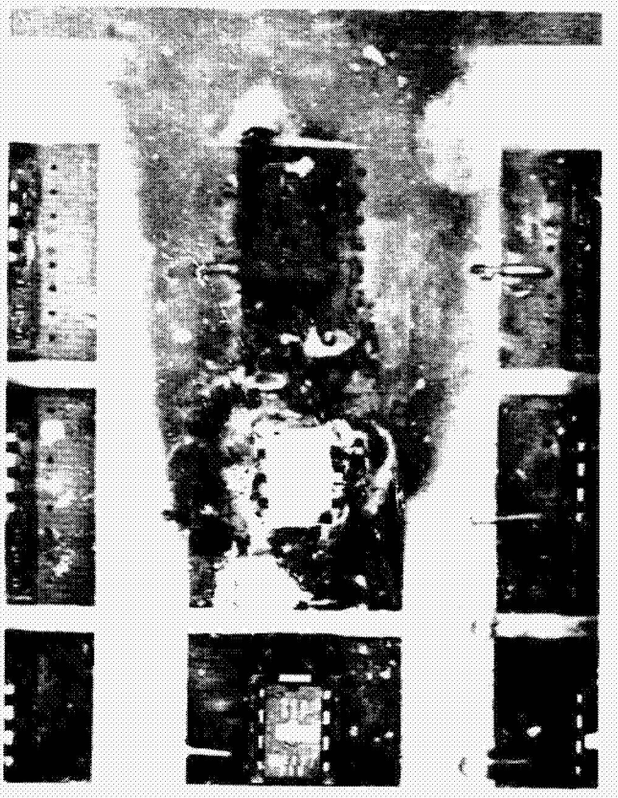
4.3.4 Group 207 Test Results

This group received the following environmental stresses

1000 Temperature cycles from -55°C to +150°C
M2
2 days operating life at 1.09 mm Mercury (vacuum life)
M3
1000 hours operating life at +5°C
M4
1000 hours operating life at +125°C
M5

The TTL parts experienced no valid failures at any time during the test.

The CMOS parts did not experience any failures until the final cell, 1000 hours operating life at +125°C. Electrical measurement at that time (M5) showed four Mfr. E and six Mfr. C parts failed.



Linear 741
Manufacturer C
Cause of Failure: Thermal Runaway, conbustion of encapsulant and massive electrical failure.

Figure 4-32 Group 206 Gold-Metallized Linear 41 Failure: Thermal Runaway

4.3.4 Group 207 Test Results (Continued)

In Mfr. E, two of the failures were caused by channeling of the n-channel transistors in the manner previously described for other test groups. One failure resulted from a shorted gate oxide region. Failure analysis attempts at locating the failure site were unsuccessful. The final failed Mfr. E part was found to have a cracked die in addition to blown metallization on several pins as seen in Figure 4-35. Since it was not possible to determine if the cracked die caused the electrically abusive currents to flow or if the cracked die was merely incidental to the abuse symptoms, this failure is counted as a valid failure. It is postulated that the cracked die occurred during temperature cycling but did not cause electrical disruption until the 125°C operating life test.

The Mfr. C CMOS parts also experienced channeling failures: four parts showed channeling of the n-channel FETs.

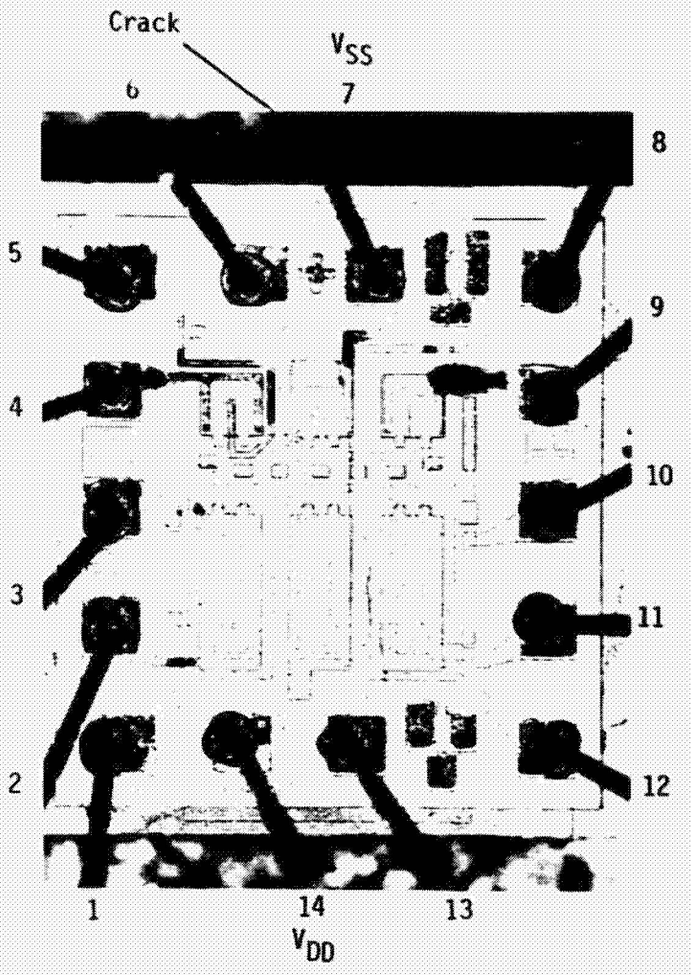
The Mfr. E 741 linear parts experienced only one valid failure in this series of environmental tests. One part (Serial Number 3950) developed a shorted MOS capacitor after the third stress increment of 1000 hours operating life at +5°C.

The failure symptom was that the Op Amp output was latched hard to the (-) supply. A curve tracer was used to confirm there was no shorted or open pins, and pin to pin voltage measurements were normal except output (pin 6) on the failed unit was latched to -12.5 volts.

The part was then decapped in hot nitric acid and visually inspected. Nothing obvious was noted (i.e. arc-over or blown metal) that would account for the output being latched low. See Figure 4-34. In order that the part could be further electrically tested the part was remounted in a 14 pin Dip package and the leads reinstalled. Bench tests showed the output to still be latched low. When the part was then set up and electrically probed, the MOS capacitor was found shorted. While attempting to measure the short resistance the capacitor rehealed. The part was then bench tested again and found functional, but was erratic. The part was then put into the SEM under bias in an attempt to find the capacitor failure site using voltage contrast. However, before any data could be taken the part went from erratic to a hard failure (output latched low). The part was then removed from the SEM and the MOS capacitor reprobed, and it was found to be a 800Ω short.

4.4 Summary of Test Failures and Interrelationships

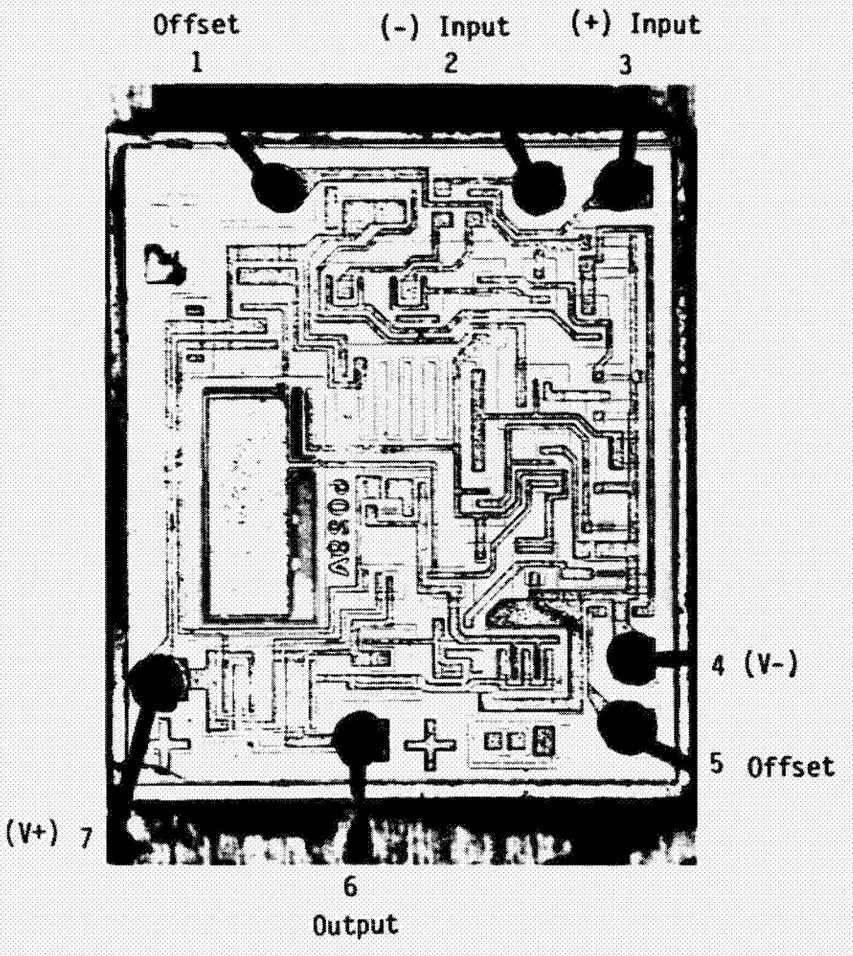
Channeling: A large number of the CMOS devices failed due to channeling or high leakage inputs. These failures occurred whenever any kind of high temperature operating life test was used: group 201, increment 4; group 206, increments 1, 2, and 3; and group 207, increment 4. It was determined that this channeling failure mechanism derives from impurities in the CMOS surface oxide rather than from impurities resident in the epoxy encapsulant. However, the impurities in the oxide could have migrated there from the adjacent epoxy encapsulant.



75X

CMOS 4007
Manufacturer E
Serial Number 2531
Cause of Failure: Cracked die and electrical abuse
Previous Environmental Stress: 1000 Temperature cycles, -55°C to +150°C; 2 days Vacuum life, 1000 hours Operating Life at +5°C and +125°C.

Figure 4-33 Group 207 CMOS Mfr. E Failure: Cracked Die and Electrical Abuse



Linear 741
Manufacturer E
Serial Number 3950
Cause of Failure: Shorted MOS capacitor
Previous Environmental Stress: 1000 Temperature cycles from -55°C to +150°C, 2 days Vacuum Life, 1000 hours Operating Life at +5°C.

Figure 4-34 Group 207 Linear 741 Mfr. E Failure: Shorted MOS Capacitor

4.4 Summary of Test Failures and Interrelationships (Continued)

Gold-Aluminum Bond Degradation: A new failure mechanism (called "plastic plague") for gold-aluminum bonds was observed in this program. Normal Kirkendall diffusion at the gold-aluminum interface apparently proceeds far beyond the normal diffusion because the bond is held in place by the compressive epoxy encapsulant. Bond failure does not occur as early under these conditions since the ball bond is not free to lift off the pad. Failures of this type were observed in Group 201, increment 2, and Group 206, increments 1, 2, and 3. In all cases these were stresses that involved exposure to elevated temperatures for extended time periods.

Other more conventional bond failures due to peripherally open ball bonds were observed during temperature cycling which exposed the parts to elevated temperatures for extended time periods. These peripheral opens resulted from degradation and voiding of the aluminum bond pad around the periphery of the ball bond with the actual ball bond retaining its mechanical integrity.

The conclusion from these bond failures is that while the epoxy encapsulant did not contribute to the generation of the failures, the use of epoxy encapsulant requires the use of gold wires to withstand the injection molding stresses and this means gold-aluminum bond degradation is very likely to be present in epoxy encapsulated microcircuits.

Temperature Cycling and Broken Wires: Temperature cycling induced large numbers of failures due to broken wires, but mostly only at the very severe limits of the environmental stress. One manufacturer, Mfr. C, did experience failures at lower stress levels but even these were at cumulative stress levels above those that usually cause failure in hermetic parts with aluminum lead wires. One manufacturer (Mfr. A) experienced only one broken wire in the entire test program. It should be pointed out that many of the broken wire failures were only observed during electrical measurement at 125°C. Of the 156 broken wire failures 25 (or 18%) were observed only at +125°C electrical measurement, indicating that the predominant failure mechanism of pre-novolac encapsulated microcircuits (hot-intermittent-opens) might be a problem with novolac encapsulated microcircuits that are temperature cycled. This was the only place where hot intermittent opens occurred however, and only after extremely severe thermal cycling, leading to the conclusion that novolac encapsulated microcircuits have the capability to withstand the thermal cycling environment with high integrity.

Ruptured Encapsulant: All parts placed on 200°C operating life test experienced the surprising failures of swollen and deformed encapsulant that broke wires loose inside the package. This puts a positive constraint on the temperature at which operating life or accelerated stress tests can be conducted. Apparently in exceeding the claimed glass transition temperature of 175°C for a long time period, the epoxy degrades violently. Thus all future accelerated life tests must be limited to a +175°C maximum, which will require extended time periods to achieve statistically significant numbers of failures.

4.4 Summary of Test Failures and Interrelationships (Continued)

Thermal Runaway: The linear devices (gold metallized 741 op amp) experienced severe problems of thermal runaway when subjected to operating life tests at +150°C. Solutions to this problem lie either in revised burn-in circuits in the MIL-spec or in a different device design capable of surviving this relatively low operating temperature. Limitation of the 741 op amp to +125°C operating life tests appears necessary but imposes problems of extremely long test times at 125°C, since no failures occurred in any of the three cells operated for 1000 hours at 125°C (Group 201, increment 4; Group 206, increment 1; and Group 207, increment 4).

Absorbed Moisture: Four CMOS parts experienced failures after moisture resistance (humidity cycling) tests that have been attributed to absorption of moisture in sufficient quantities to disrupt the CMOS operating currents (Mfr. E) or even allow excessive and destructive test currents to flow (Mfr. C). It is postulated that this absorption occurred in the plastic rather than in the silicon die itself, and that it was accelerated by the prior stress of 15 cycles of thermal shock. The Mfr. E failures all recovered after bake out, and since no bias was applied during humidity cycling, channeling could not have been induced. Thus the bake out is assumed to have driven out the absorbed moisture. For the Mfr. C CMOS part, electrical abuse failure occurred before bake out so no improvement could be observed.

These failures of CMOS parts after humidity cycling casts severe doubts on the ability of epoxy encapsulated CMOS parts to withstand humidity environments. Further testing is highly desireable to obtain better resolution of the problem.

Freak Failure: A small number of failures occurred for reasons not related to the environmental stress applied. The group 206 M3 Mfr. B TTL diffusion short, the group 207 M5 Mfr. E CMOS cracked die and gate oxide short, and the group 207 M4 Mfr. E Linear 741 shorted MOS capacitor all fall into this category. This is a total of four parts out of 2275 parts tested and is seen to be an extremely small number of freak failures.

Stress Corrosion Cracking: Only one manufacturer's parts experienced stress corrosion cracking, even though all five manufacturers parts were handled in an identical manner and three other manufacturers' parts were located in the same environment at all times. Since the activation energy of this failure mechanism could not be determined under the conditions of this test, it is not known what the likelihood is of stress corrosion cracking occurring at lower temperatures.

Epoxy encapsulated microcircuits are basically uncontrolled parts with no possibility of control by the user over processes used by the manufacturer. For this reason the only way to ensure that devices to be used in systems are free from stress corrosion cracking would be to institute a lot acceptance test that would reveal the possibility of the occurrence of stress corrosion cracking.

5.0 PROCUREMENT AND APPLICATION CONSIDERATIONS

5.1 Design, Application, and Processing Constraints

The results of the program show that novolac encapsulated microcircuits can be used in a wide variety of system applications if certain constraints are applied to their use. These constraints differ for the three circuit technologies evaluated: TTL, CMOS, and linear.

5.1.1 TTL Constraints

The exceptionally good performance of the TTL devices was marred only by the occurrence of stress corrosion cracking with the Manufacturer A parts. Because of the uncontrolled nature of plastic encapsulated microcircuit production, no processing controls can be applied economically to suppliers to ensure avoidance of this problem. Further understanding of the problem might show that it is unique to only silver plated lead processing, in which case the only constraint necessary is avoidance of silver plated lead devices.

In general, however, some form of lot acceptance test is indicated to ensure that stress corrosion cracking problems do not surface with other manufacturer technologies as a result of the constant and rapid uncontrolled processing changes made in the encapsulated microcircuit market. This lot acceptance philosophy is discussed below.

From the packaging design and manufacturing stand point, it appears that great care should be taken to avoid exposure of at least silver plated Alloy 42 leaded devices to salt contamination, since the chloride ions present could breach the plating and attack the Alloy 42 lead material, resulting in stress corrosion cracking.

The only other constraint that appears significant with TTL devices is the need to avoid exposure to temperatures greater than 175°C to avoid the ruptured encapsulant mechanism observed after 1000 hours at 200°C. Since typical system application device temperatures are generally kept below 125°C and preferably below 75°C, this does not impose a severe constraint on widespread application of TTL encapsulated microcircuits to space system applications.

5.1.2 CMOS Constraints

The major problem encountered with CMOS devices was channeling. There was a significant difference noted between the two manufacturers in terms of percentage of devices that channeled, but this difference probably varies from week to week for any one manufacturer's production.

In any event, both manufacturers' CMOS parts did demonstrate channeling under 125°C operating life tests, which means that this is not a suitable upper limit for device operation. A more desireable upper limit is probably 70°C, unless a specific test and analysis is made by the user of a particular CMOS manufacturer's current product to ensure that channeling will not occur at higher temperatures.

5.1.2 CMOS Constraints (Continued)

An additional constraint on the CMOS devices is the desireability of avoiding exposure to humidity cycling unless the user verifies by testing that a particular design is impervious to humidity cycling in his application.

5.1.3 Linear Constraints

The linear devices appear to be susceptible to thermal runaway when operated at temperatures above 125°C. This could result from elevated device junction temperatures caused by higher power operation or it could be merely caused by basic instabilities in the thermal design of linear microcircuits. In any event it appears that a thorough thermal characterization should be made of any linear microcircuit which must operate of elevated temperatures approaching 100°C ambient. With this exception, there do not appear to be any constraints on the general application of encapsulated gold metallized linear microcircuits to space applications.

5.2 Qualification Test Considerations

Because of the nature of the manufacturing and sale of encapsulated microcircuits at extremely low costs, manufacturer-performed qualification testing is not likely to be an accepted mode of operation with manufacturers. User-performed qualification tests must then be instituted to assure the integrity of the parent population from which any specific lot of parts is selected. Two types of qualification testing should be performed: initial device qualification and lot acceptance qualification.

It is apparent that the rapid turnover in processing technology for encapsulated microcircuits would render any attempts at periodic qualification-retention meaningless: lots delivered immediately after requalification testing could deviate dramatically from the lots on which the qualification testing was performed.

5.2.1 Initial Qualification

The initial qualification procedure should be intended to determine the basic integrity of the manufacturer's product over a wide range of device types using the same package configuration. For this reason, extensive high stress testing should be performed to search for systemic flaws in the basic product. The test seen to be most revealing for this evaluation is the 175°C 1000 hour operating life test. This test would be very effective in identifying the following areas of device vulnerability.

- o Channeling of CMOS microcircuit
- o Stress corrosion cracking of external leads
- o Degradation of gold-aluminum bonds

Thus failure analysis of the fall out from this test is an important adjunct to the test itself in identifying weak or failure prone process technologies.

5.2.1 Initial Qualification (Continued)

Humidity life test per MIL-STD-883 Method 1004 is also felt to be necessary in initial qualification to ensure that the device electronics are not susceptible to the possible ingress of minute amounts of moisture.

In both cases, the actual environmental stress test should be preceded and followed by 100% tri-temperature (-55°C, 25°C, 125°C) electrical measurement.

Other degradation test methods commonly used for qualification testing (such as vibration, thermal cycling, centrifuge, etc.) are felt to be non-productive in evaluating the integrity of encapsulated microcircuits. The package mechanical tests commonly used such as solderability and lead bend should be retained, with particular emphasis on performing lead bend after the 175°C 1000 hour operating life to search for stress corrosion cracking.

It should be pointed out that the 175°C temperature must be avoided with linear microcircuits unless it can be verified that the operating power dissipation is low enough that junction temperature will stay within safe limits. If a lower temperature operating life test is used for linear microcircuits, the time should be extended beyond 1000 hours if at all possible within the schedule allowances, to compensate for the reduced temperature.

5.2.2 Lot Acceptance Qualification

Each lot of encapsulated microcircuits received by a user should be subjected to degradation testing using high stress techniques on a sample of the lot. The preferred lot qualification test would be 160 hours operating life at 175°C with tri-temperature electrical testing performed before and after the life test. A small number of the parts should then be subjected to lead bend testing to search for possible stress corrosion cracking. Standard sampling procedures and accept/reject criteria should be used.

Post-mortem analysis of any failures is very important to ensure that systemic problems have not been introduced by recent manufacturing process changes. This will ensure also that freak failures are not misinterpreted as being indicative of basic manufacturing flaws.

5.3 Screening Test Considerations

In keeping with the motivation for use of encapsulated microcircuits, namely low cost, the screening procedures should be restricted to low cost tests that produce the maximum likelihood of intercepting a defective part or potential defective part.

The recommended screening test for use with encapsulated microcircuits is 100% electrical measurement at -55°C, 25°C, and +125°C. If possible both ac and dc parameters should be measured, but at least the dc parameters should be measured at all three temperatures. It was seen from this test program that die-related failure mechanisms were almost completely eliminated from the failures generated by the environmental stress tests. This is attributed to the 100% tri-temperature electrical measurement that was performed following burn-in.

5.3 Screening Test Considerations (Continued)

Other stress test programs performed on microcircuit parts in the past (4, 5) have also employed burn-in but electrical measurement was made only at 25°C, and the subsequent failures under environmental stress have uncovered numerous die-related failures. This indicates that the burn-in screen is not responsible for the interception of die-flaw failures : the tri-temperature electrical measurement itself is the key screen test for intercepting infant mortality parts or "part that never worked".

This is borne out by system level thermal testing performed by Boeing during proof testing of SRAM electronic systems. Fahley (6) found that the high and low temperature system testing was uncovering numerous parts with defects that had not been intercepted by burn-in followed by 25°C electrical measurement. When high and low temperature electrical measurement was added to screening of the parts, the system thermal-test failure rate due to microcircuit die-related causes dropped to zero.

For traditionalists who feel that burn-in itself is a "must", the 100% tri-temperature measurement could be followed by a 160 hour burn-in at 125°C, followed by another 100% tri-temperature electrical measurement. The 125°C 160 hour burn-in is so far from the basic Arrhenius curve for modern microcircuits that its use is considered harmless.

Other screen tests studied in this program are felt to be either meaningless when applied at the low stress levels affordable on a 100% basis, deleterious to useful device life time if carried to accelerated levels, or valueless in terms of accelerating epoxy-unique failure mechanisms.

6.0 ADDITIONAL STUDY AND EVALUATION AREAS

6.1 Introduction

The study performed under this contract has resulted in the definition of several additional areas that should be investigated. These areas result from the specific findings of the study in regard to certain failure mechanisms; from inconclusive results from certain environmental stress tests; and from the fixed time increments for the operating life tests. The three areas that should be studied further are:

- Evaluation of the efficacy of JAN Level B screening tests (particularly thermal cycling and burn-in) in rejecting freak parts, with emphasis on complete thermal characterization (tri-temperature electrical measurement) prior to thermal cycling, prior to burn-in and following burn-in.

- Evaluation of the failure causes in screened and unscreened parts when subjected to high temperature operating life tests for logarithmic time increments.

- Extended humidity life testing (both biased and unbiased) with the test continued long enough to cause significant failures.

The result of these investigations would give answers to the specific question:

- If certain specific screening or qualification tests are performed on encapsulated microcircuits, how good will the surviving parts be for space applications.

6.2 JAN Level B Screening Evaluation

MIL-STD-883 Method 5004.2 Level B calls for certain specific environmental and operational stress tests to be performed on microcircuits. However there is no callout of electrical measurements to be made at -55°C and +125°C until the completion of burn-in. Thus devices which do not ever function correctly at +125°C can pass through stabilization bake, thermal cycling, interim electrical parameter measurement (25°C) and burn-in with the final electrical measurement being the first time the failure is detected. Based on the results of this program, it appears that the -55°C, 25°C, +125°C electrical measurements intercepted all bulk and surface pinhole failures prior to environmental stress testing but it is not possible to determine which stress test made the defect show up.

The desired study program would subject representative TTL and CMOS parts to the same sequence of environmental tests but would make -55°C, 25°C, 125°C electrical measurements before and after every stress increment. Failure analysis on all rejects would identify the type of failure mechanism each stress uncovers.

The result of this study would be a definition of alternative screening methods to those called out in Method 5004.2 which would be significantly lower cost, thus salvaging the low cost advantages of encapsulated microcircuits. In particular, the value of the tri-temperature electrical measurement itself would be defined as a possible substitute for the tests called out in Method 5004.2.

6.3 High Stress Tests on Screened vs. Unscreened Parts

All parts subjected to environmental stress testing on this program were screened to MIL-STD-883 Method 5004.2, Level B. This screening and subsequent rejection of defective devices tended to dilute the impact of the high stress tests. In addition, the high stress tests were performed for long increments of time with few intermediate measurements, making an accurate measurement of median-time-to-failure impossible.

The desired study program would resolve these problems by performing high stress tests on parts which receive no screening except tri-temperature (-55°C, 25°C, 125°C) electrical measurement, as well as on parts subjected to full screening as described in paragraph 6.2. The high stress tests would then be conducted at logarithmic time intervals, e.g. 1 hour, 3 hours, 10 hours, 30 hours, etc. until enough failures occur to determine the log normal failure distributions, sigmas and median-times-to-failure. The use of multiple stress cells rather than step stress cells would also permit determination of the Arrhenius relationships for each failure mechanism found.

6.4 Extended Humidity Life Testing

The only humidity life testing performed in this program was one cell of 10 day humidity life per MIL-STD-883 Method 1004. Very few failures occurred and these failures were somewhat inconclusive.

The desired study program would subject screened and unscreened parts to extended humidity cycling under both biased and unbiased conditions. The humidity cycling would be continued with tri-temperature electrical measurements made at either linear or logarithmic increments of number of cycles, until a large percentage of each device type in each cell failed. Failure analysis of the failed devices would be performed to categorize the predominant failure mechanisms and determine the true ability of encapsulated microcircuits to survive humidity cycling.

7.0 References

1. Jack Q. Reynolds, "Effects of Sustained Temperature Cycling on Parts", 1968 Reliability and Quality Control Symposium Proceedings, pp. 486-493.

2. M. R. Carpenter, W. Fitch, "Thermomechanical Testing Techniques for Microcircuits - Final Technical Report", RADC TR-75-134, May 1975.

3. D. D. Robinson, W. A. Finke, P. A. Lindberg, "Preventive Maintenance of Electronic Systems - Phase I Final Technical [illegible]t" Boeing Document No. D180-12863-1, April, 1971.

4. H. Sello, I. Blech, "Some New Aspects of Gold-Aluminum Bonds", Journal of the Electrochemical Society, Vol. 113, No. 10, October, 1966.

APPENDIX A

CONSTRUCTION ANALYSIS

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APPENDIX A1

CONSTRUCTION ANALYSIS

TTL 5400/7400 DEVICES

Manufacturer A
Manufacturer B
Manufacturer C
Manufacturer D

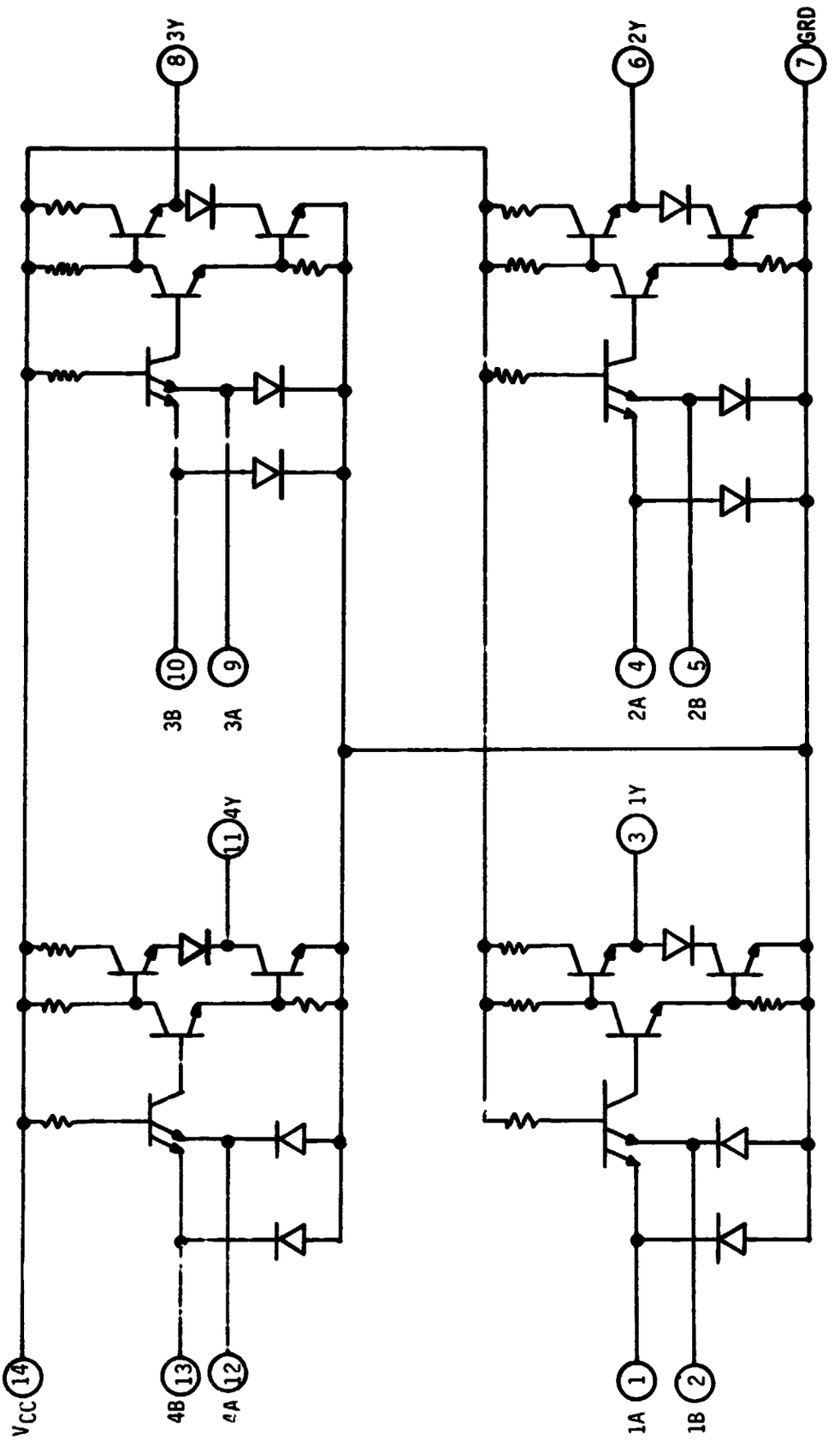


Figure A-1. TTL 5400/7400 Schematic

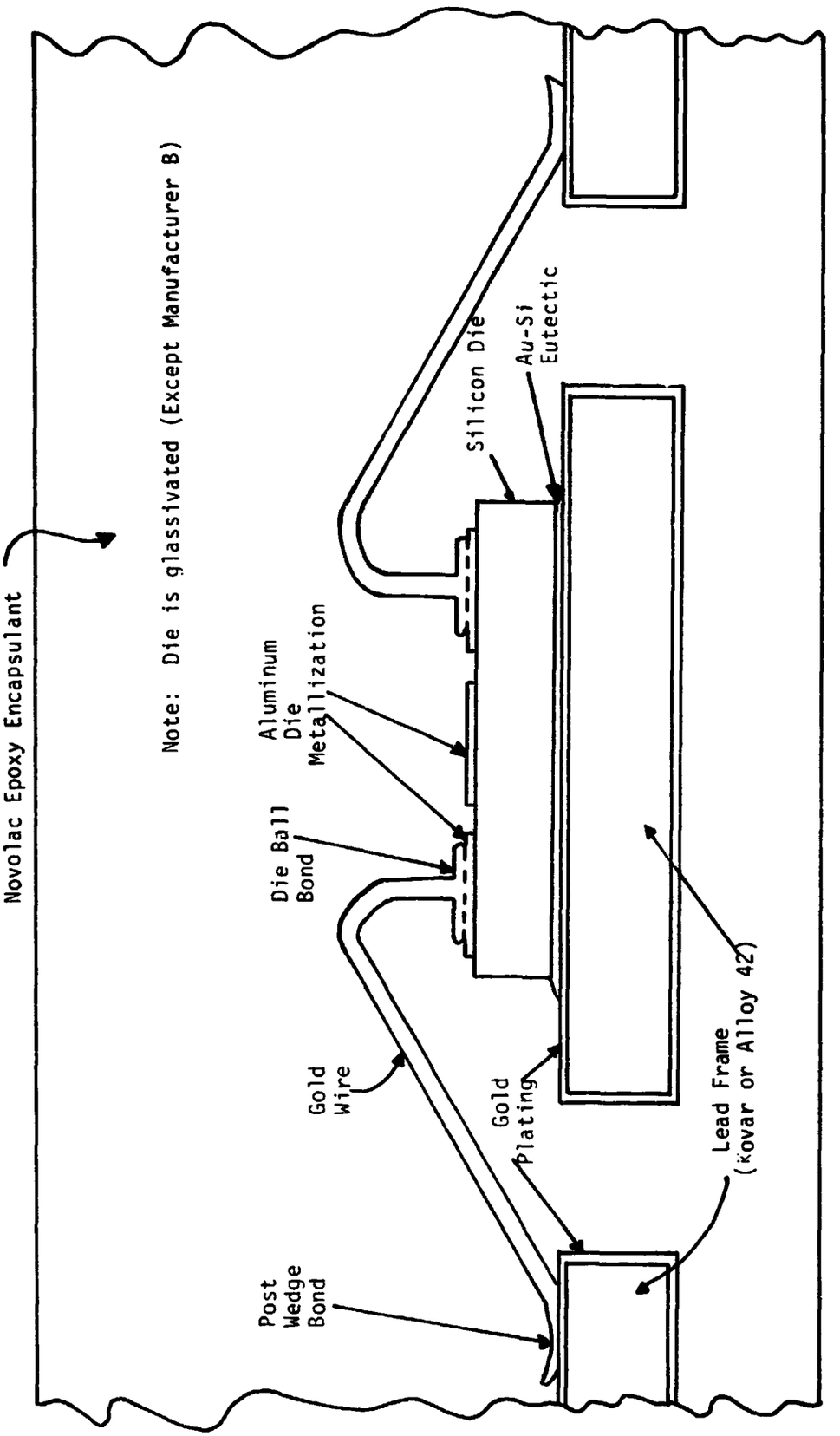
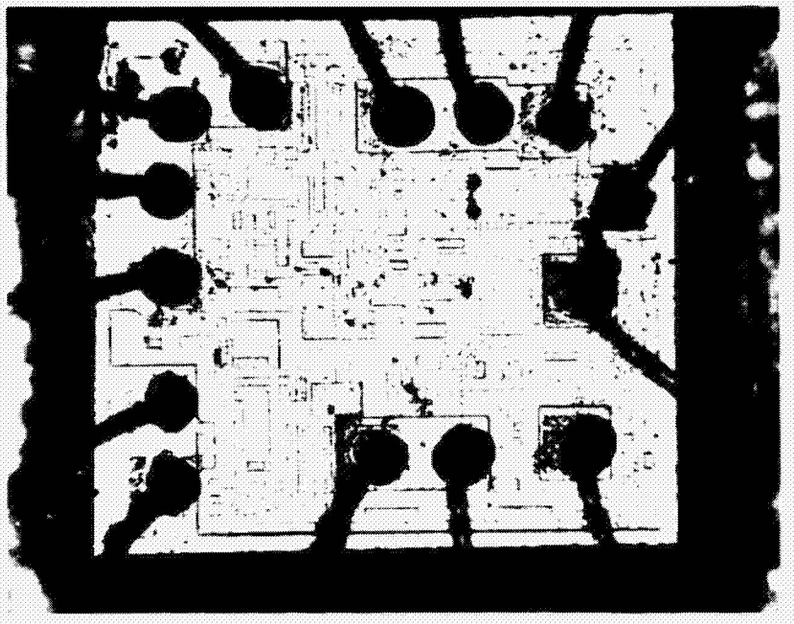


Figure A-2. Construction Details: Manufacturers A, B, C, D TTL (and Manufacturer C CMOS)

MFR. CODE	DATE CODE	LEAD FRAME MATERIAL	LEAD FRAME PLATING	INTERNAL LEAD WIRE	DIE METAL	DIE ATTACH METHOD	JUNCTION COAT	ENCAPSULANT (NOVOLAC)
A	7410	Alloy 42 (Hi-Nickel Alloy of Iron)	Silver-150µin. min	1 mil Gold TC Bond	Al	Eutectic. Bare Si-Back. Au-Si-Ag Preform	None	Proprietary - Custom spec to 3 large suppliers. Not Commercially available.
B	7407	Alloy 42	Gold. 30µin. min.	1 mil Gold TC Bond	Al	Eutectic. Bare Si-Back. No Pre-form.	None	Epoxy B
C	508/ 511	Alloy 42	Gold	1 mil Gold TC Bond	Al	Eutectic. Bare Si-Back. No Pre-form.	None	Epoxy B
D	7425	Kovar	Tin 300µin. min.	1 mil Gold TC Bond	Al	Eutectic. Gold Back Die. No Pre-form.	None	Morton 410B

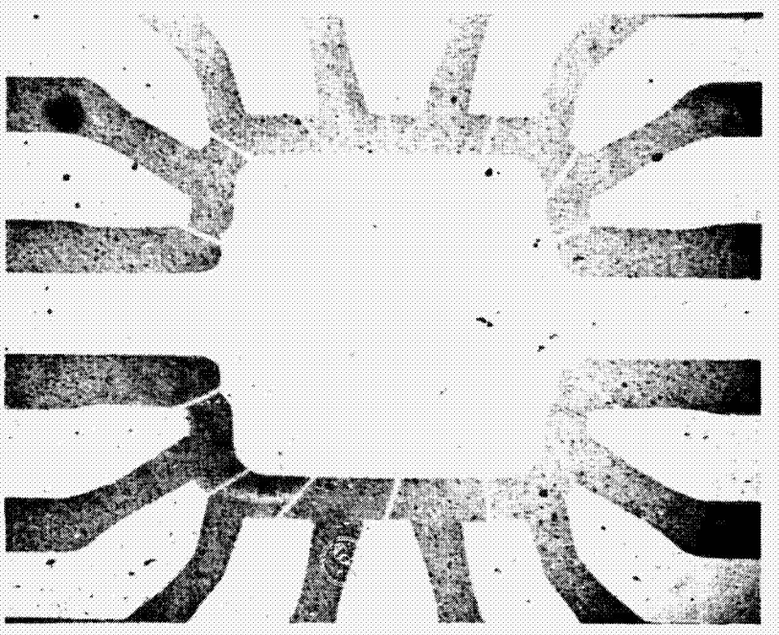
FIGURE A-7. TTL 5400/7400 CONSTRUCTION DETAILS



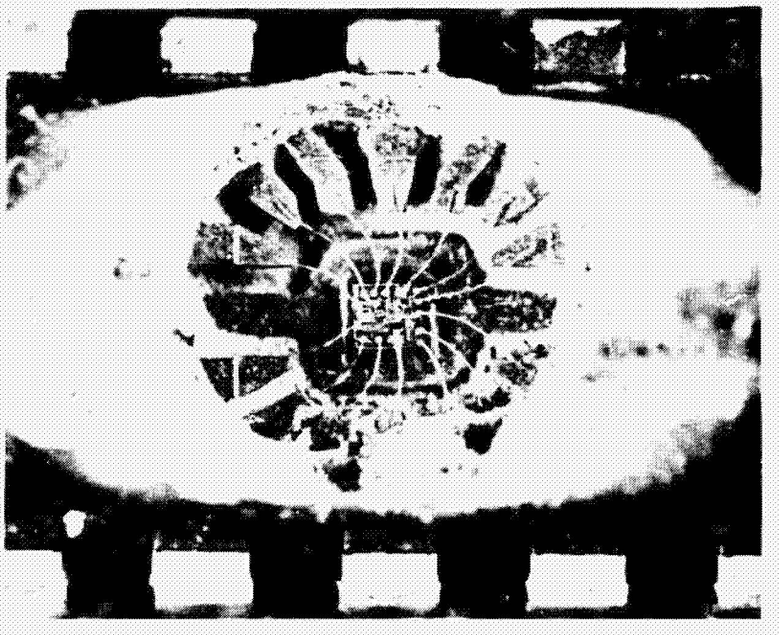
Photograph of Die

Note: Residue on die is a result of chemical stripping of the encapsulant.

Figure A3. Manufacturer A TTL 7400 Construction Analysis

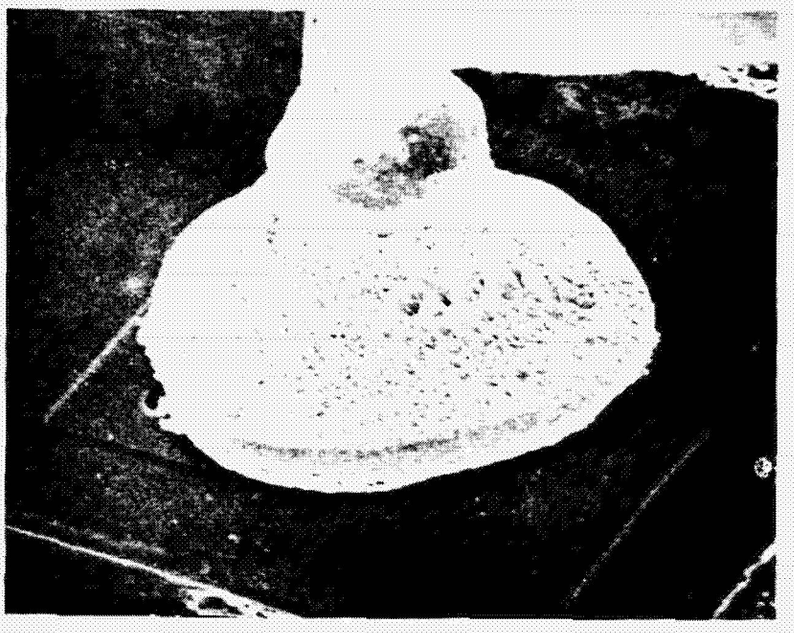


X-Ray of Lead Dress (Before Opening)



Photograph of Die and Lead Dress
Note deformation of lead wires caused by injection molding.

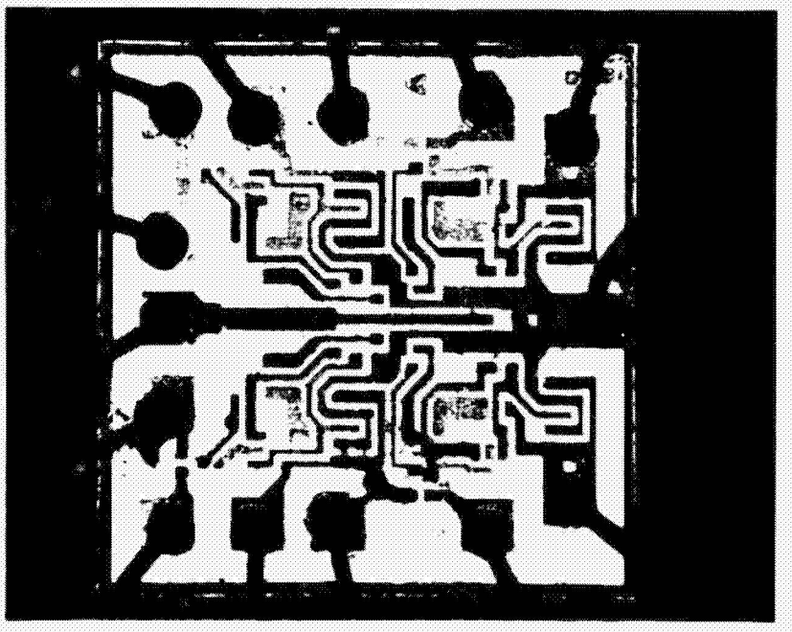
Figure A3. (Continued) Manufacturer A TTL 740



SEM Photo of Ball Bond 700X
Note: Removal of encapsulant also removed aluminum bonding pad.

SEM Photo of Oxide Window and Step Coverage 2000X

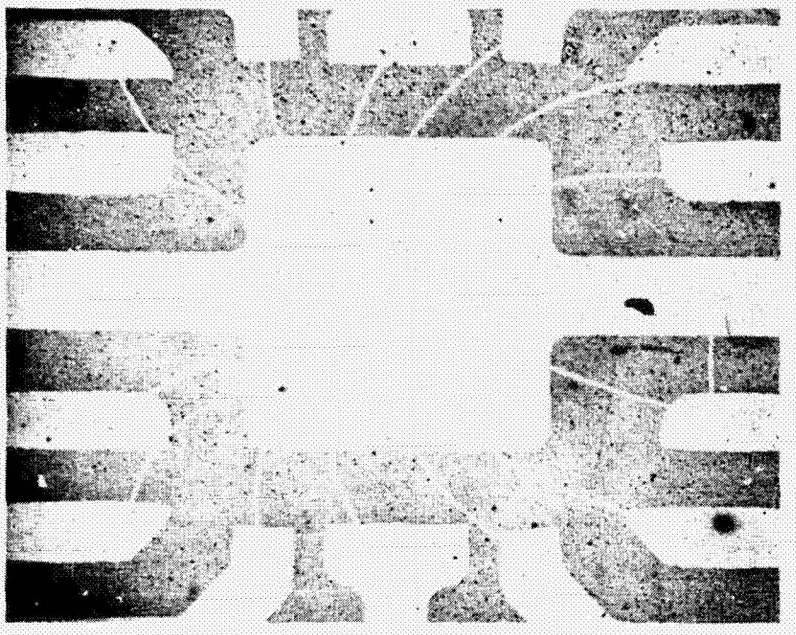
Figure A3 (Continued). Manufacturer A TTL 7400



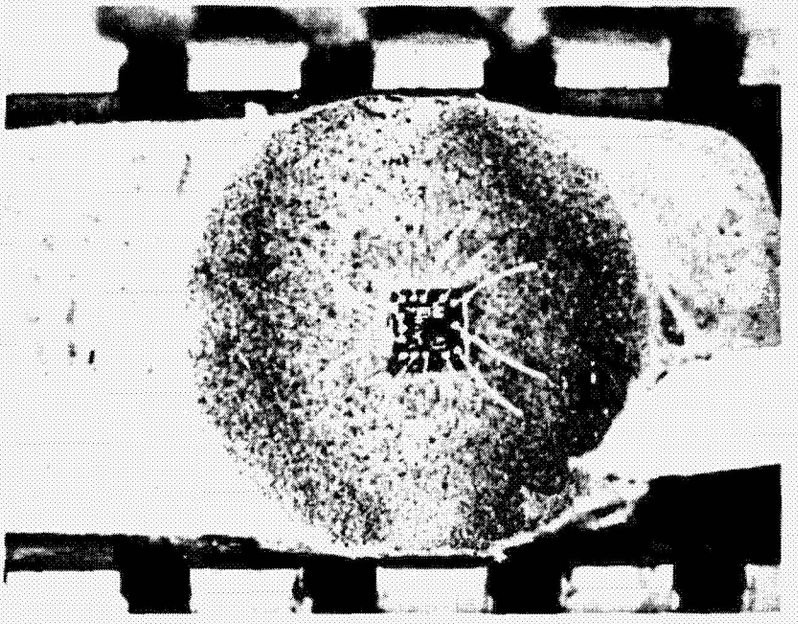
Photograph of Die

Note: Die was not glassivated, hence chemical removal of encapsulant attacked the aluminum metallization

Figure A4. Manufacturer B TTL 5400 Construction Analysis

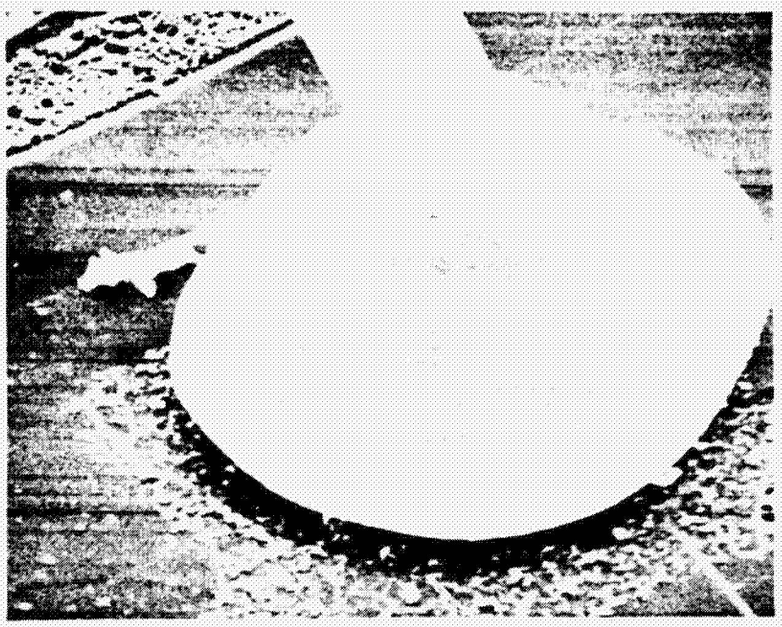


X-Ray of Lead Dress (Before Opening)



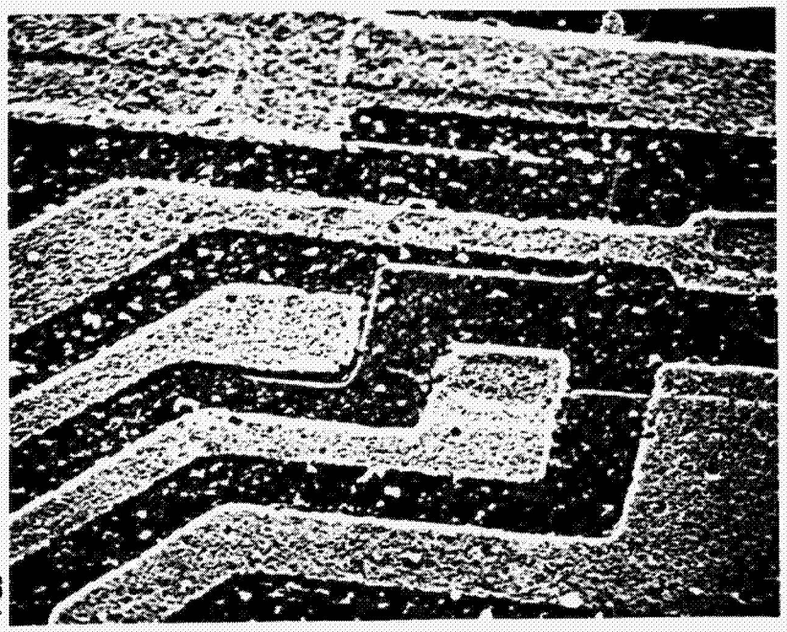
Photograph of Die and Lead Dress
Note deformation of wires due to injection molding

Figure A4 (Continued). Manufacturer B TTL 5400



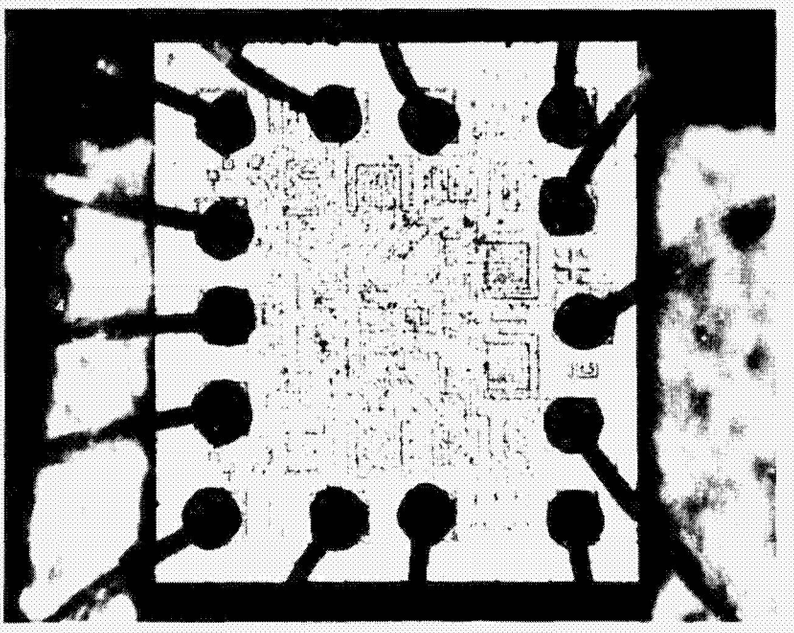
SEM Photograph of Ball Bond 700X

Note: Chemical removal of encapsulant also removed aluminum bonding pad.



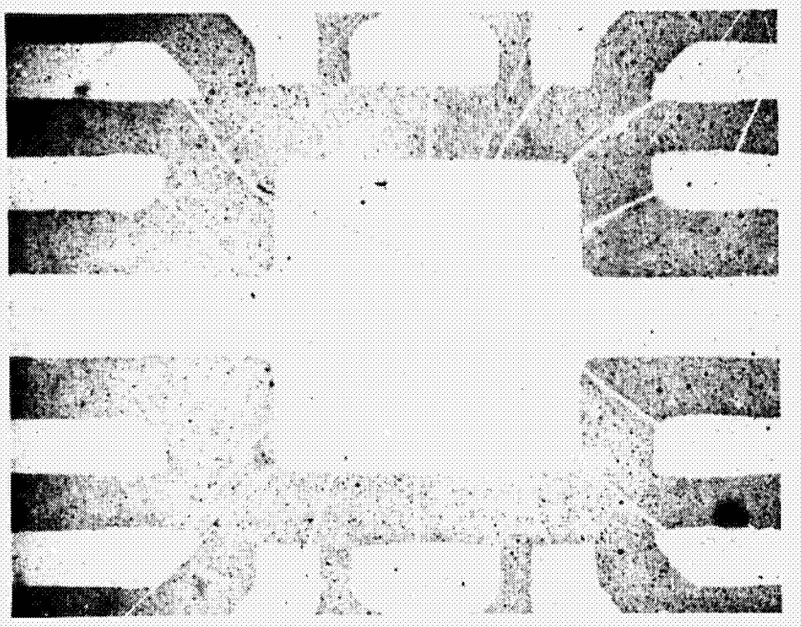
SEM Photograph of Oxide Windows and Steps 700X

Figure A4 (Continued). Manufacturer B TTL 5400

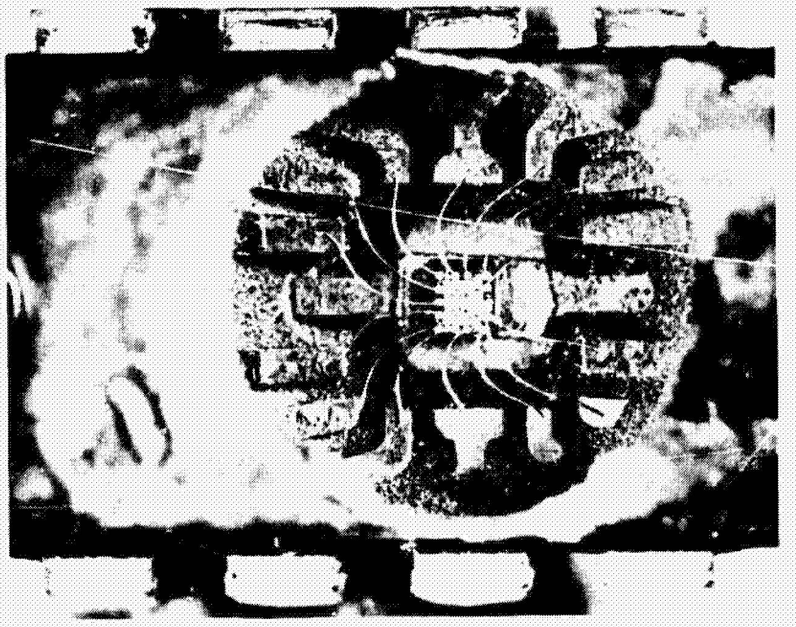


Photograph of Die

Figure A5. Manufacturer C TTL 5400 Construction Analysis

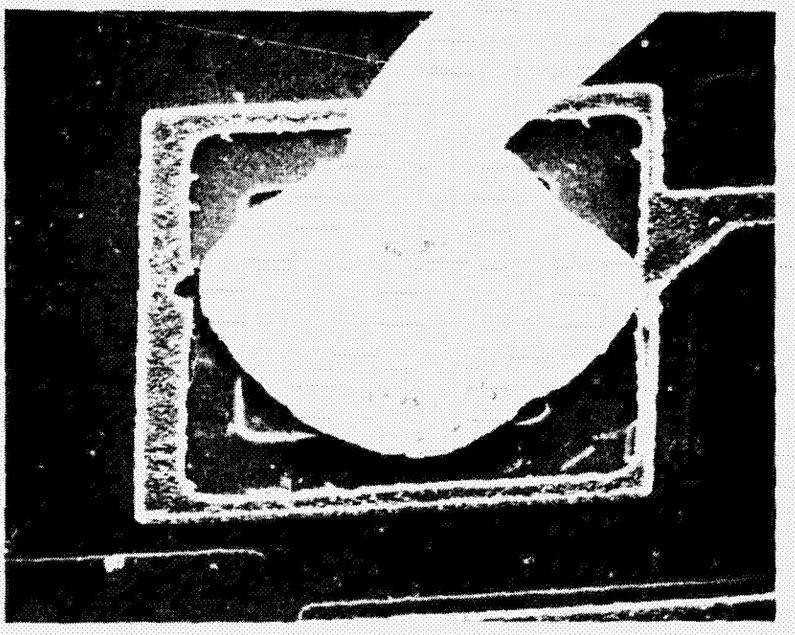


X-Ray of Lead Dress (Before Opening)



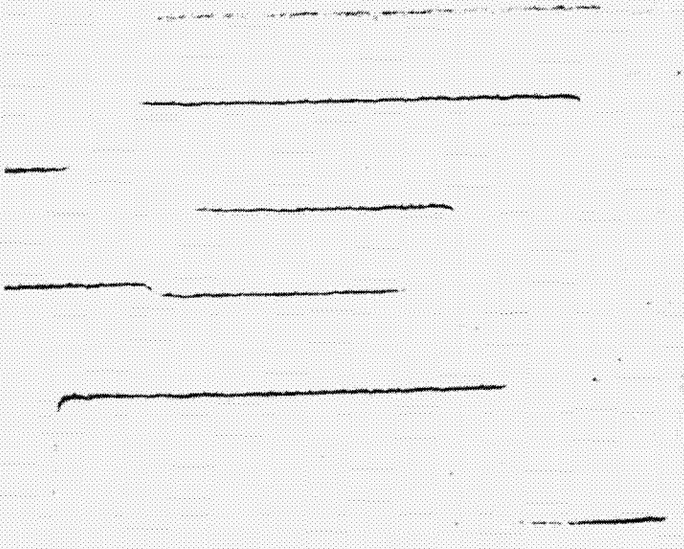
Photograph of Die and Lead Dress
Note deformation of wires due to injection molding

Figure A5 (Continued). Manufacturer C TTL 5400



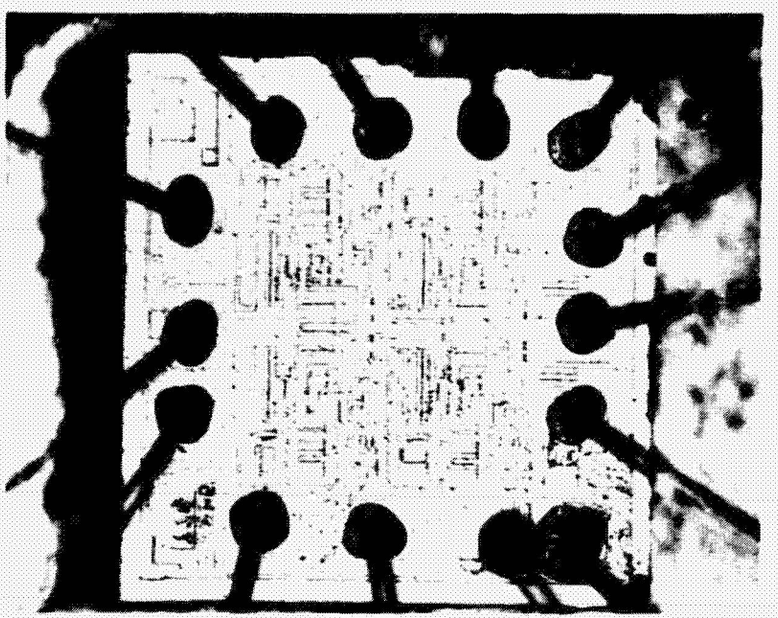
SEM Photograph of Ball Bond 700X

Note: Chemical removal of encapsulant also removed aluminum bonding pad.



SEM Photograph of Oxide Windows 700X

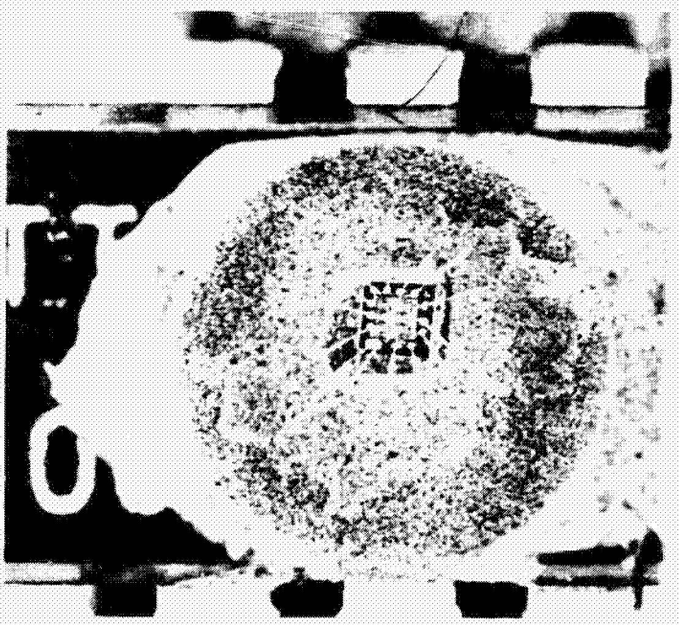
Figure A5 (Continued). Manufacturer C TTL 5400



Photograph of Die

Figure A6. Manufacturer D TTL 7400 Construction Analysis

X-Ray of Lead Dress Before Opening

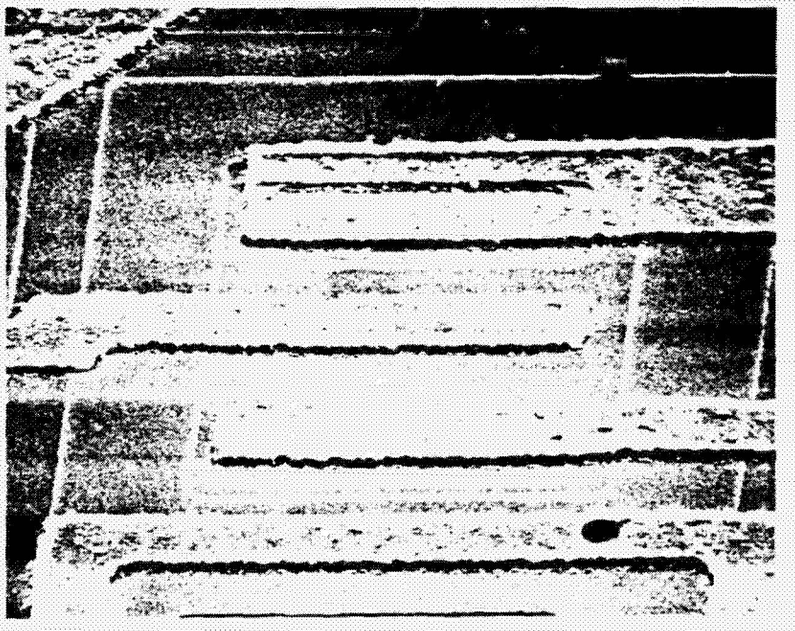


Photograph of Die and Lead Dress

Figure A6 (Continued). Manufacturer D TTL 7400

SEM Photograph of Ball Bond 700X

Note: Chemical removal of encapsulant also removed aluminum bonding pad.



SEM Photograph of Oxide Windows 1000X

Figure A6 (Continued). Manufacturer D TTL 7400

APPENDIX A2

CONSTRUCTION ANALYSIS

CMOS 4007 DEVICES

Manufacturer C
Manufacturer E

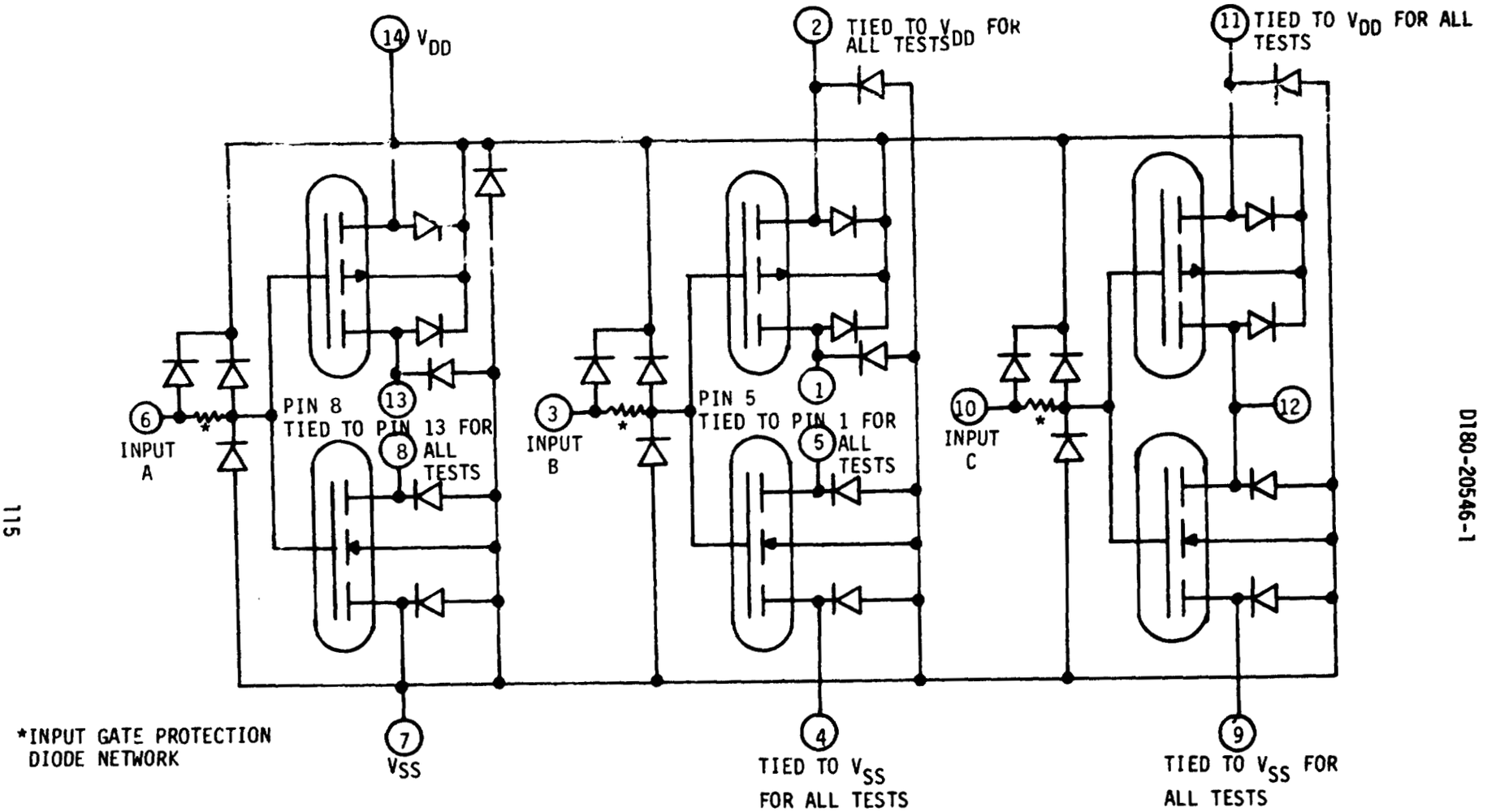
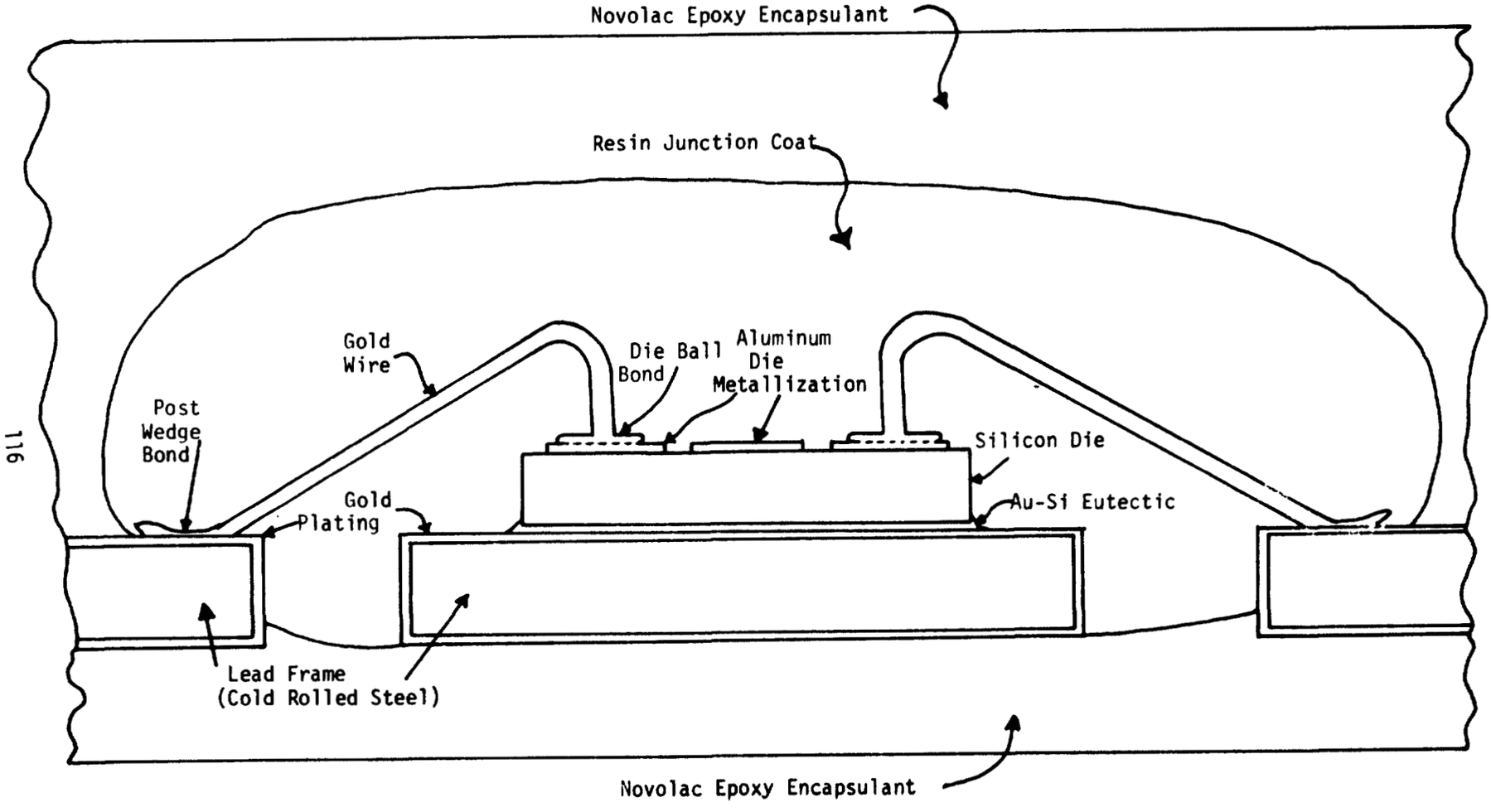


FIGURE A-8. CMOS 4007 SCHEMATIC



D180-20546-1

Figure A-9. Manufacturer E CMOS Construction Details

MFR. CODE	DATE CODE	LEAD FRAME MATERIAL	LEAD FRAME PLATING	INTERNAL LEAD WIRE	DIE METAL	DIE ATTACH METHOD	JUNCTION COAT	ENCAPSULANT (NOVOLAC)
E	444	Cold Rolled Steel	Gold Plated, Solder Dipped	1 mil Gold TC Bond	Al	Eutectic. Bare Si-Back. No Pre-form	Emerson & Cuming Resin + Catalyst + Thinner	Allied Novolac 2342
C	446	Alloy 42	Gold	1 mil Gold TC Bond	Al	Eutectic.	None	Epoxy B

FIGURE A-13. CMOS 4007 CONSTRUCTION DETAILS

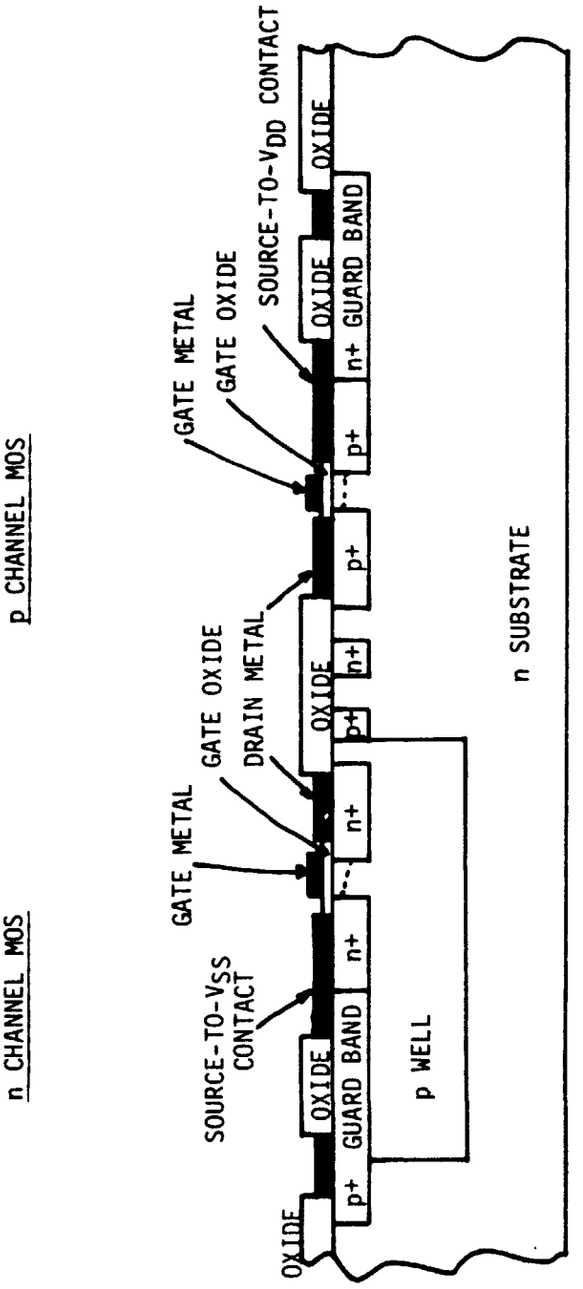
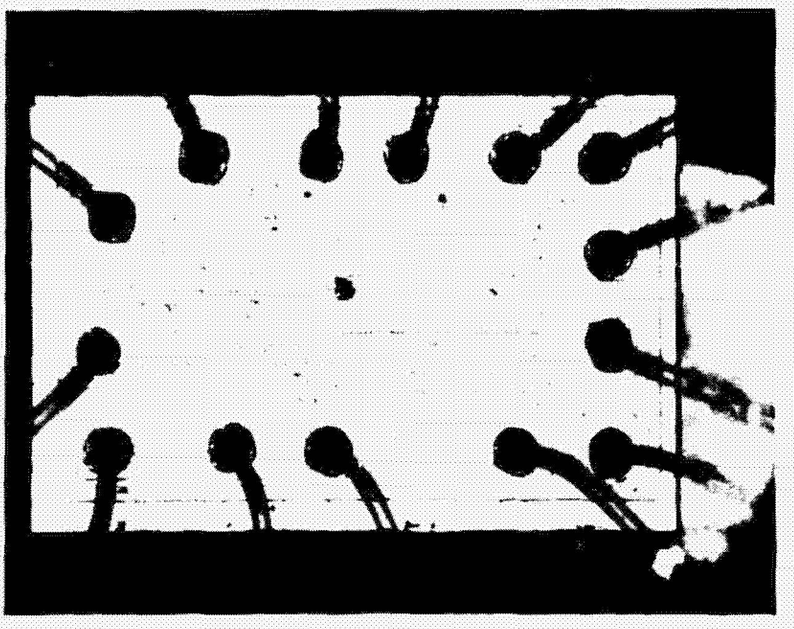
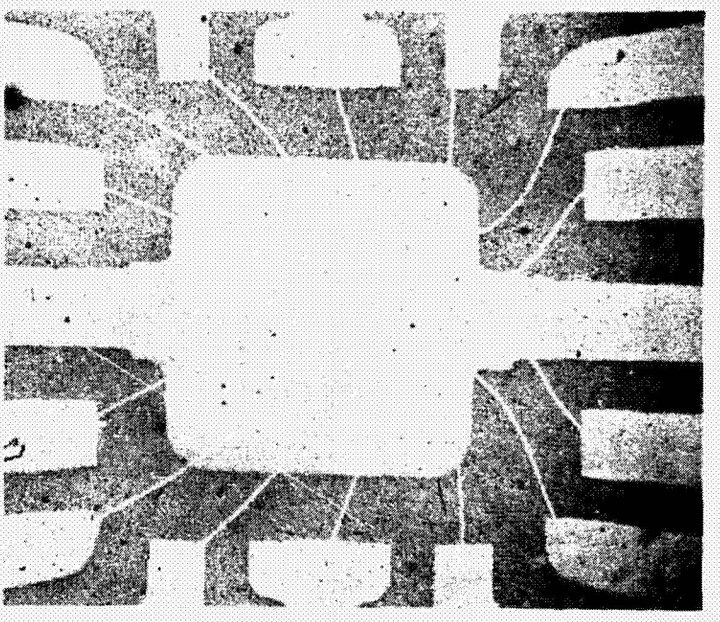


FIGURE A-10. CROSS SECTION OF CMOS STRUCTURE

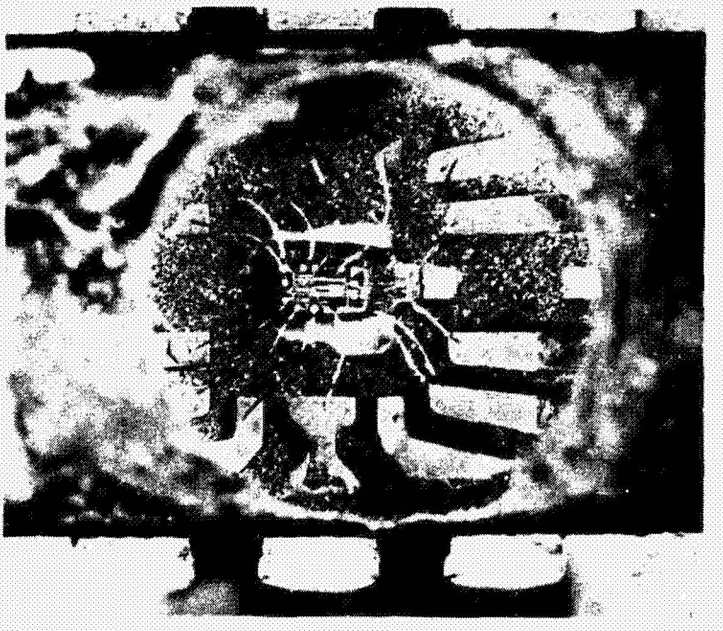


Photograph of Die

Figure A11. Manufacturer C CMOS 4007 Construction Analysis

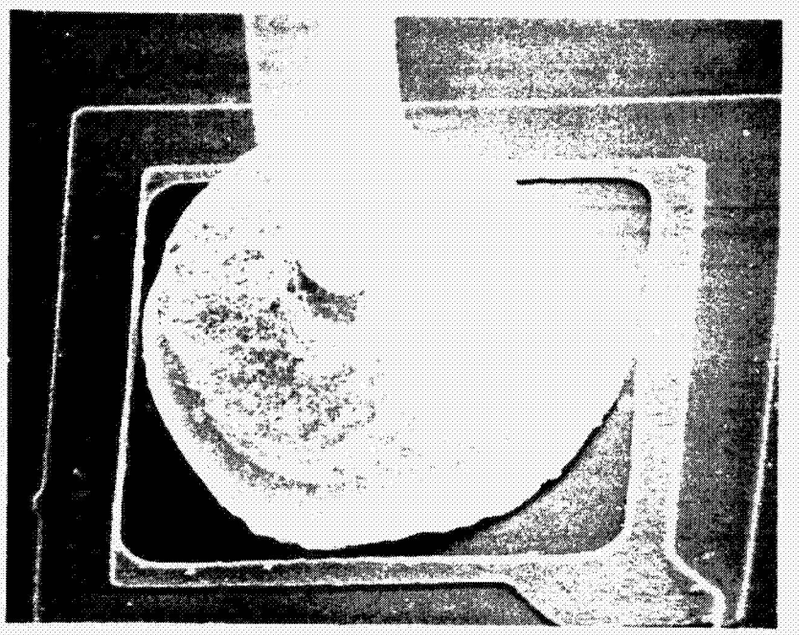


X-Ray of Lead Dress (Before Opening)



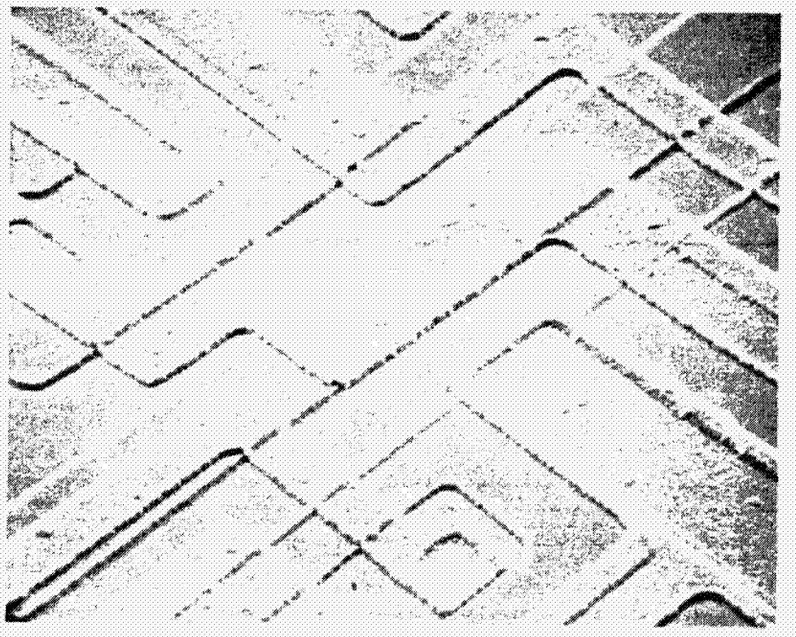
Photograph of Die and Lead Dress
Note deformation of wires due to injection molding

Figure A11 (Continued). Manufacturer C CMOS 4007



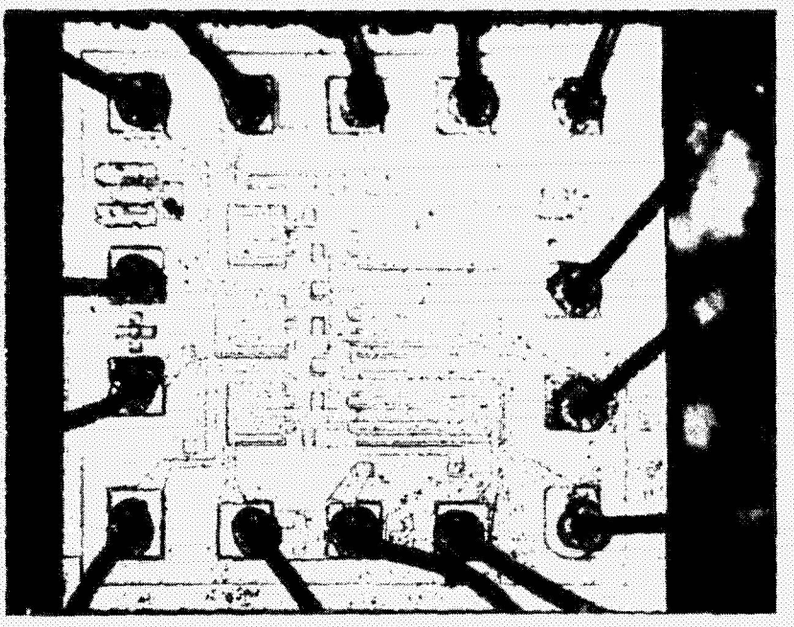
SEM Photograph of Ball Bond 700X

Note: Chemical Removal of encapsulant also removed aluminum bonding pad.

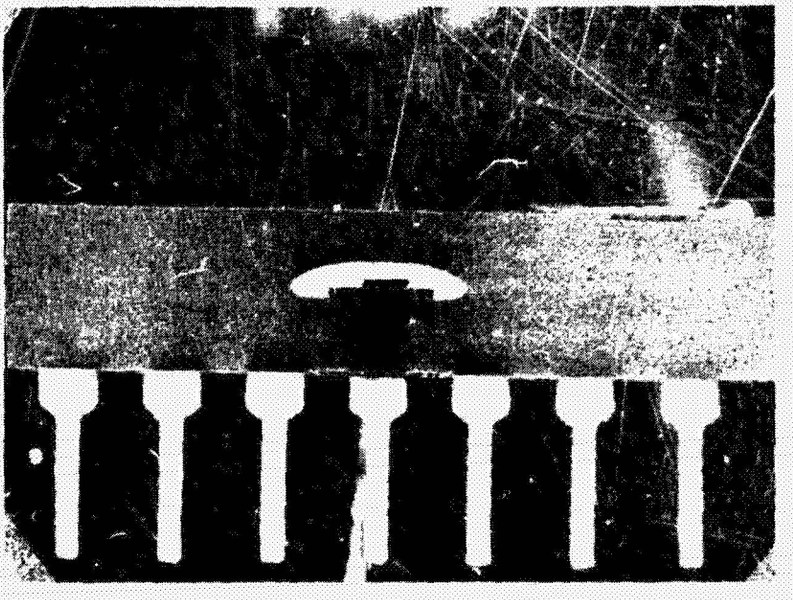


SEM Photograph of Oxide Windows and Steps 1000X

Figure A11 (Continued). Manufacturer C CMOS 4007

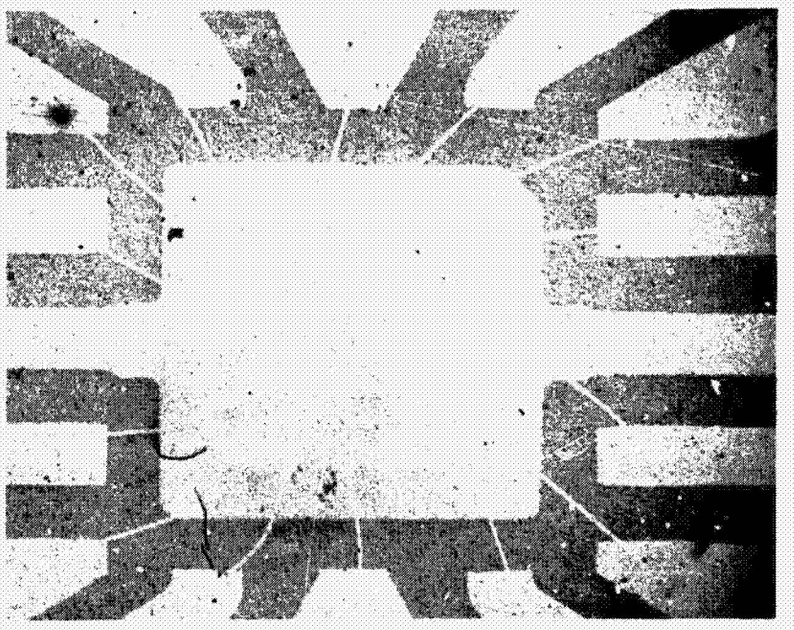


Photograph of Die

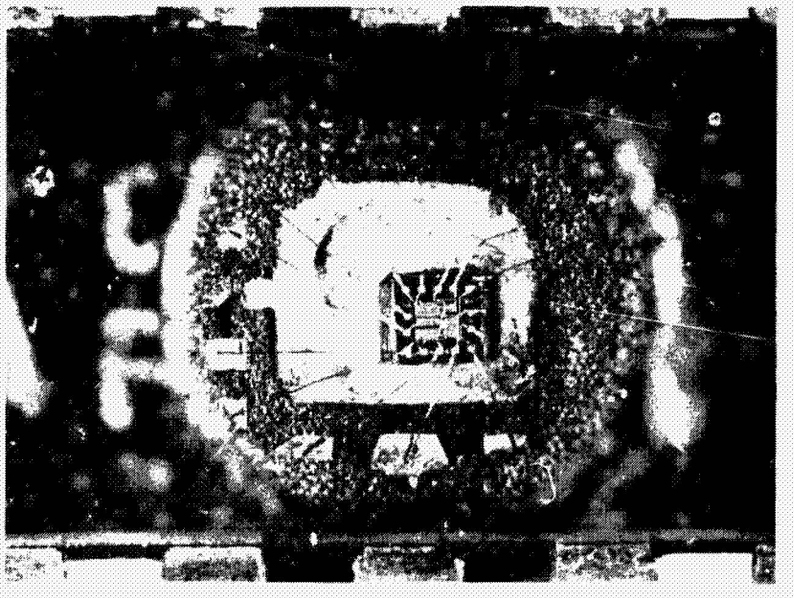


Cross Section of Device
(Note Resin Coat over Die)

Figure A12. Manufacturer E CMOS 4007 Construction Analysis

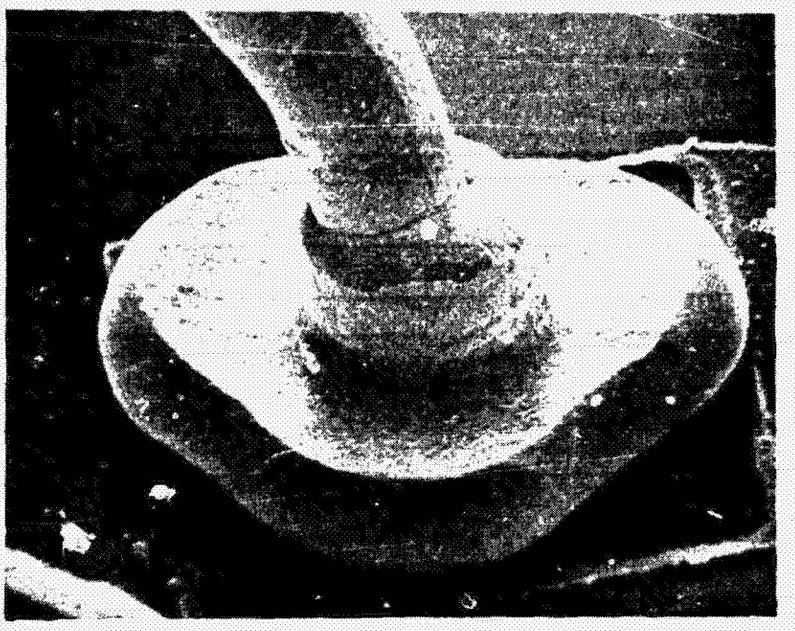


X-Ray of Lead Dress (Before Opening)

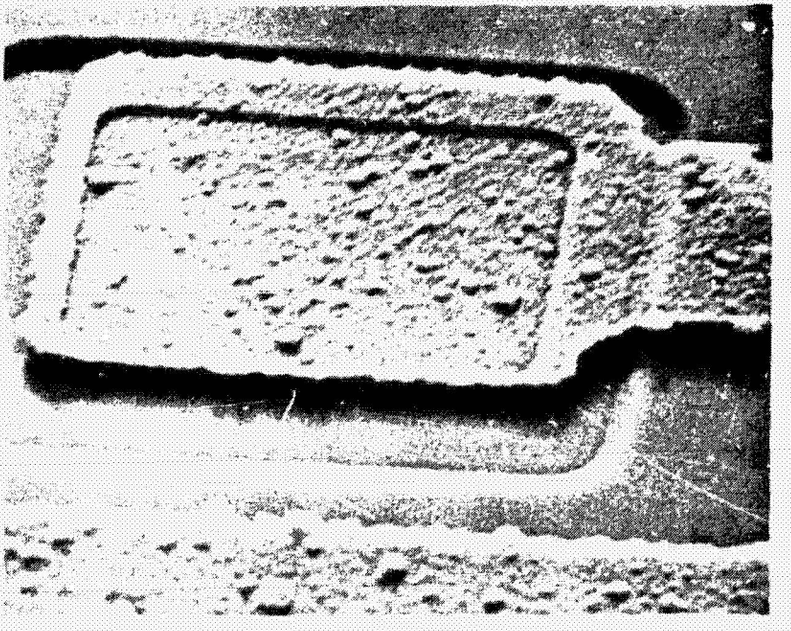


Photograph of Die and Lead Dress
Note: deformation of wires due to injection molding is not present because of resin junction coat

Figure A12 (Continued). Manufacturer E CMOS 4007



SEM Photograph of Ball Bond 700X
Note: Chemical removal of encapsulant also removed aluminum bonding pad.



SEM Photograph of Oxide Window and Steps 2000X

Figure A12 (Continued). Manufacturer E CMOS 4007

APPENDIX A3

CONSTRUCTION ANALYSIS

LINEAR 741 DEVICES

Manufacturer E

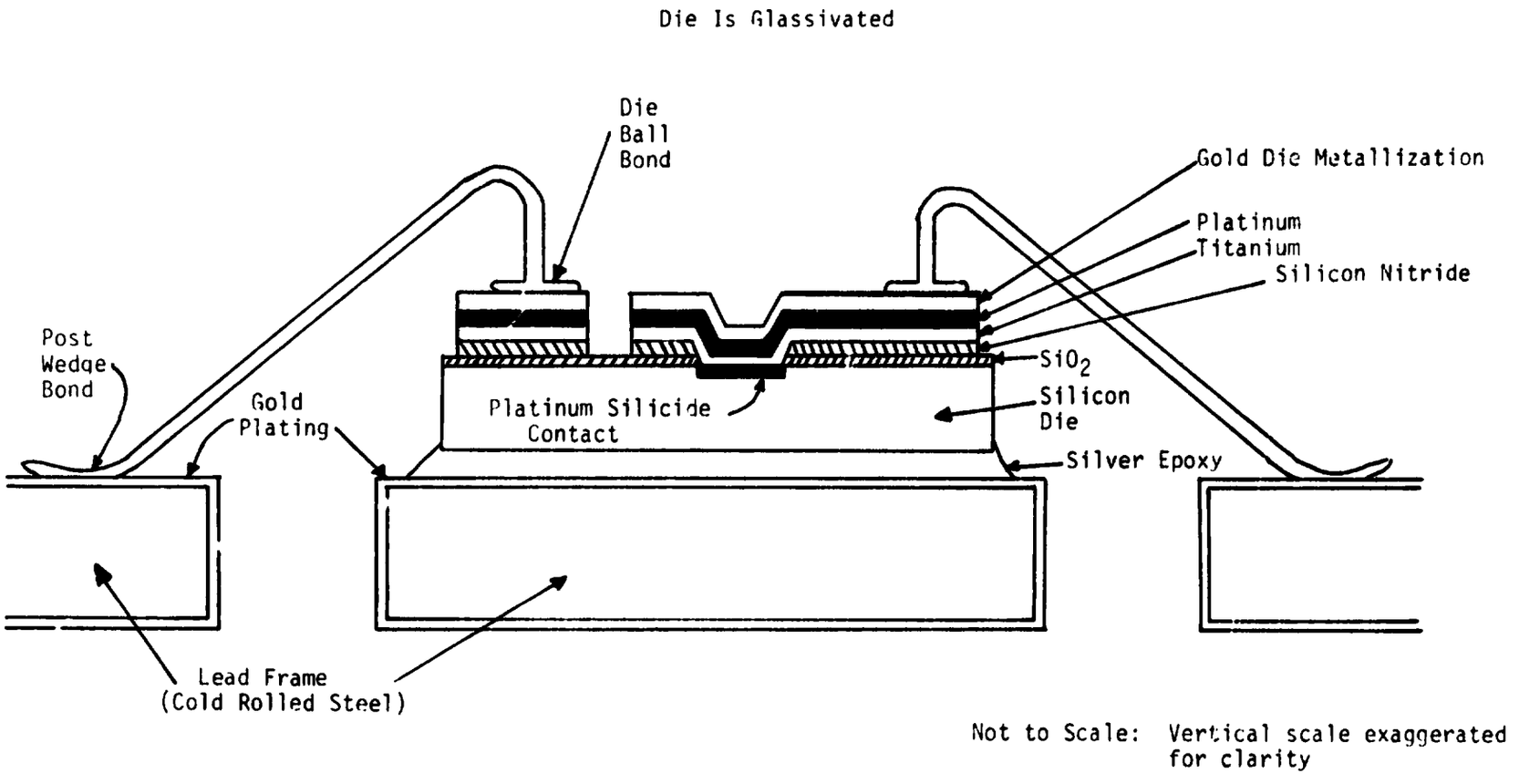


Figure A-15. Manufacturer E Linear 741 Construction Details

MFR. CODE	DATE CODE	LEAD FRAME MATERIAL	LEAD FRAME PLATING	INTERNAL LEAD WIRE	DIE METAL	DIE ATTACH METHOD	JUNCTION COAT	ENCAPSULANT (NOVOLAC)
E	527	Cold Rolled Steel	Nickel Plated, Solder Dipped	1 mil Gold. TC Bond	Ti-Pt-Au	Silver Epoxy	None	Allied Novolac 2342

FIGURE A-17. LINEAR 741 CONSTRUCTION DETAILS

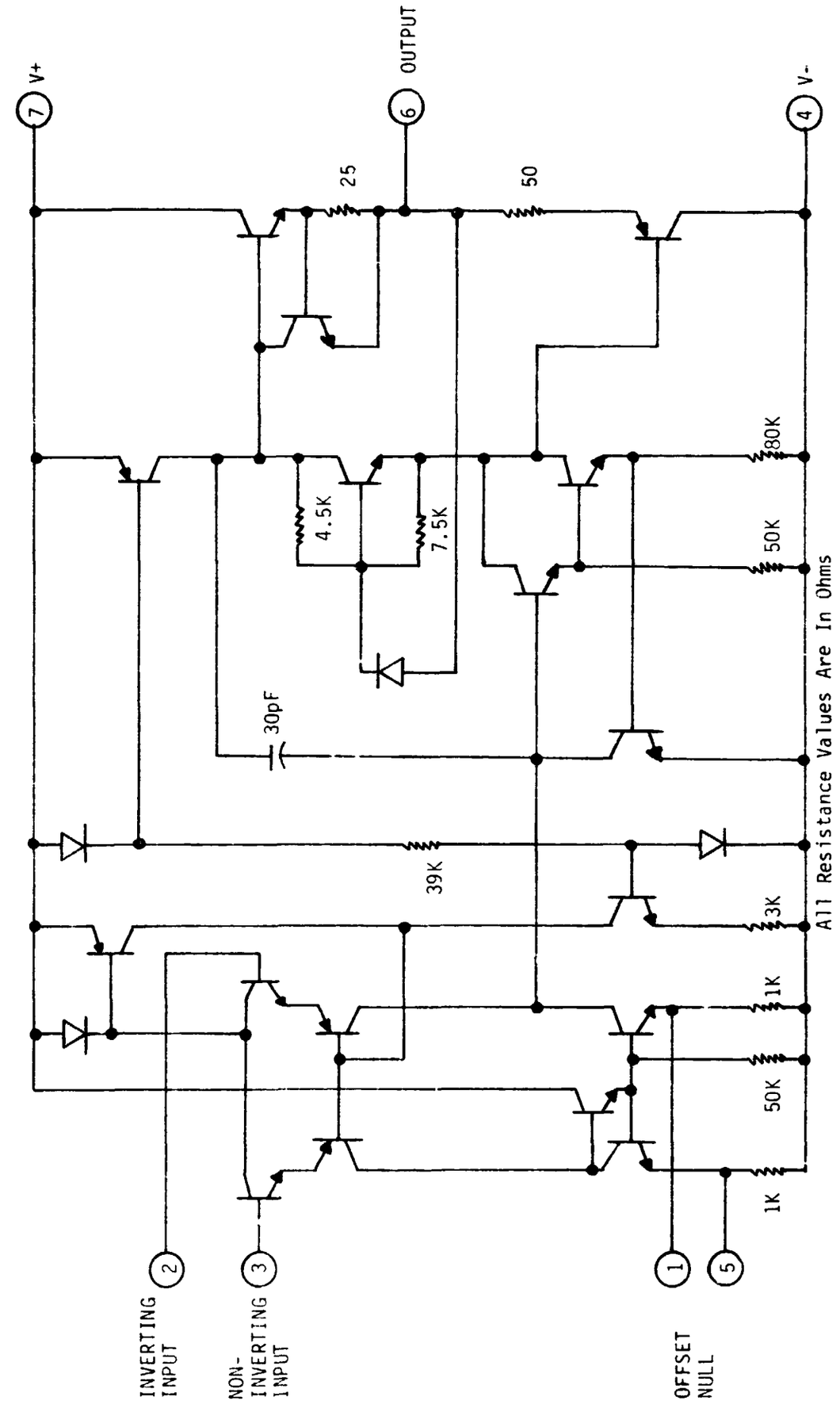
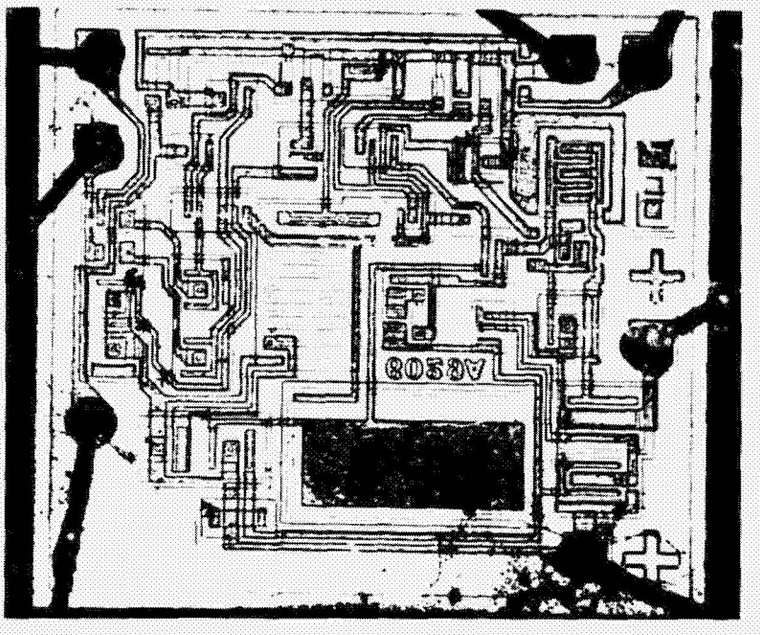
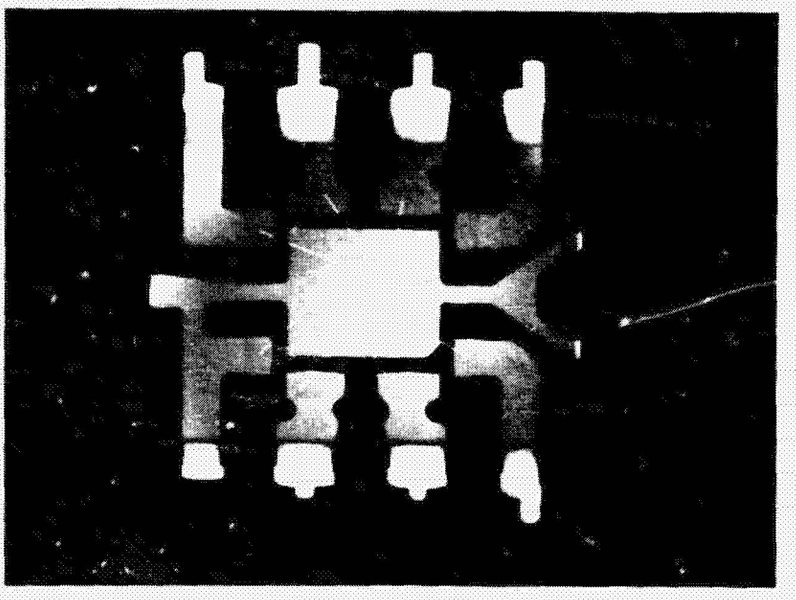


FIGURE A-14. LINEAR 741 OP AMP SCHEMATIC

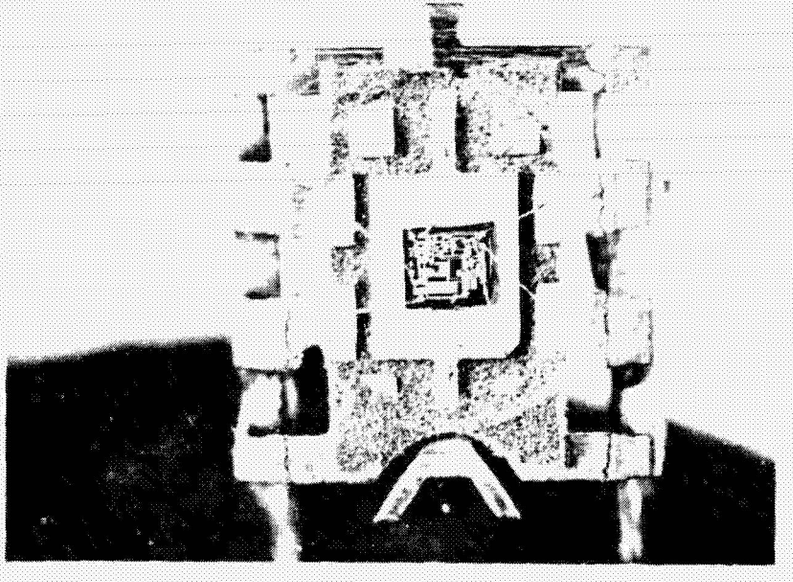


Photograph of Die 61X

Figure A16. Manufacturer E Linear 741 Construction Analysis



X-Ray of Lead Dress (Before Opening)



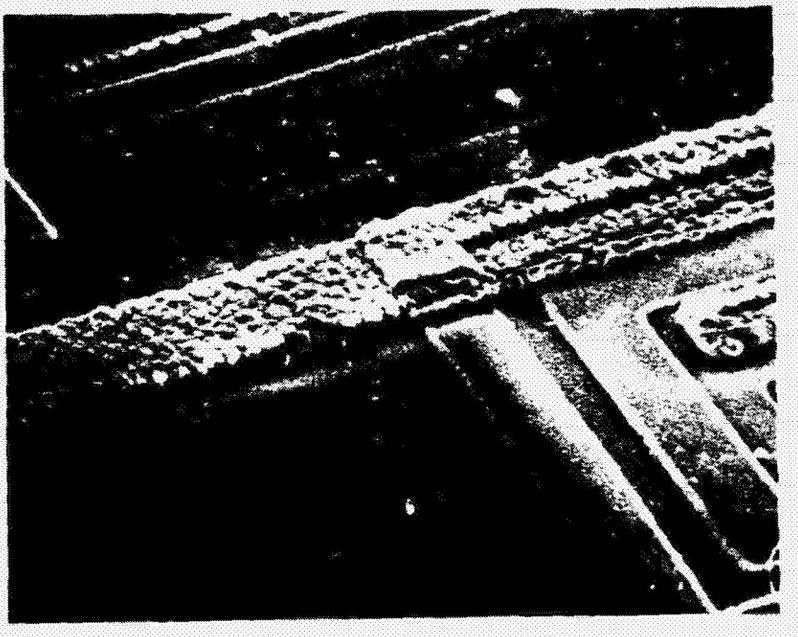
Photograph of Die and Lead Dress

Figure A16 (Continued). Manufacturer E Linear 741

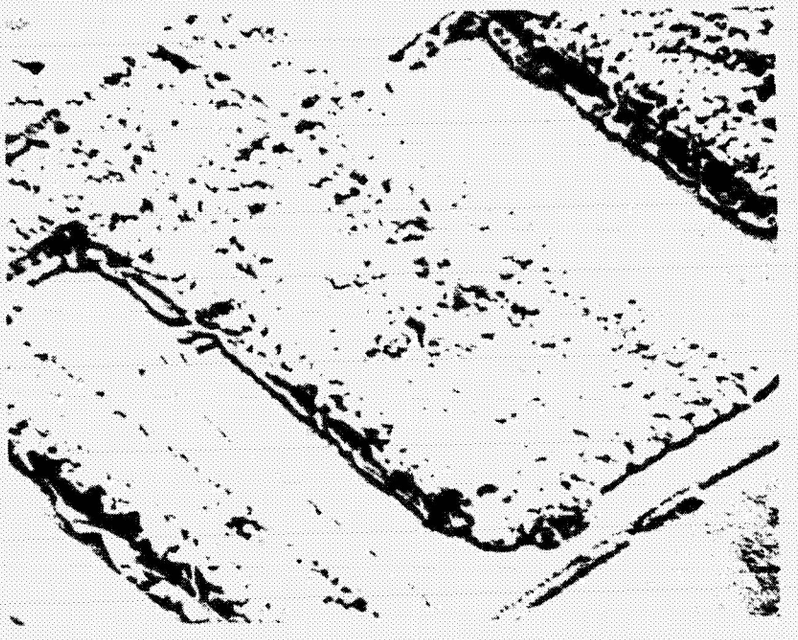
SEM Photograph of Post Bond

SEM Photograph of Ball Bond 400X

Figure A16 (Continued). Manufacturer E Linear 741



SEM Photograph of Oxide Steps 700X



SEM Photograph of Oxide Window 1000X

Figure A16 (Continued). Manufacturer E Linear 741

Appendix B

Selected Statistical Analyses

From the extremely large number of data measurements made on the microcircuits (3500 parts before stress, 2250 parts subjected to stress), a study was made of the statistical distributions of certain devices at certain stress levels to search for drifts or trends that might appear statistically but be obscured in straight forward analysis. The magnitude of the data analysis task can be appreciated by observation that this program entailed approximately 1.48 million parameter measurements. Histogram data tabulation on these parameter measurements resulted in a potential 30,000 histograms for initial and post stress data and an additional 29,000 histograms for the delta between initial and final measurements.

The approach used to resolve this massive amount of statistical data was first to combine all inputs or all outputs of a single part into one histogram. Thus for the quad 2-input NAND gate, for example, all eight input VIC parameters were combined into one histogram. Then an analysis was made of the areas in which significant changes or drifts might have occurred and only the delta deviation between initial and final measurements was plotted for these critical areas.

In Table B-1 the different series of histogram plots are shown in respect to the matrix of device types, measurement increments, and environmental stress groups.

For the TTL parts three separate series of histogram data were plotted. In Series a, histogram data on VOL, VOH, and VIC from the Manufacturer D 7400 TTL parts measured at 25°C were plotted for Group 201 at all five measurement increments: M1 initial data (pre-environmental stress) and then delta deviation data at M2, M3, M4, and M5. See Figures B-1 through B-15. In Series b, the delta deviation data after M4 was plotted for Manufacturer D parts for Groups 202, 203, 204, 205, 206, and 207 as well for the VOL, VOH, and certain VIC parameters (see Figures B-16 through B-34). In Series c, the VOL parameter measured at 25°C at M2 and M3 was plotted for Manufacturers A, B, and C. See Figures B-35 through B-40.

For the CMOS parts the same pattern was followed using 125°C measurements instead of 25°C measurements. In Series d, the parameters VOH4 and VOL2 were plotted for Manufacturer E for Group 201 M1 (initial data) and M2, M3, M4, and M5 (delta deviation data). See Figures B-41 through B-50. In Series e, the same parameters were plotted for the M4 measurements of Groups 202, 203, 204, 205, 206, and 207 for Manufacturer E.

The results of the histogram plotting showed that nothing significant occurred; even though slight drifts did occur, the drifts were generally very small compared to the magnitude of the parameter being measured.

Table B-1. Overview of Histograms Plotted

Part Type	Mfr.	Measurement	201	202	203	204	205	206	207
7400 TTL	A	M1							
		M2	c						
		M3	c						
		M4							
		M5							
5400 TTL	B	M1							
		M2	c						
		M3	c						
		M4							
		M5							
5400 TTL	C	M1							
		M2	c						
		M3	c						
		M4							
		M5							
7400 TTL	D	M1	a						
		M2	a,c						
		M3	a,c						
		M4	a,b	b	b	b	b	b	b
		M5	a						
4007 CMOS	E	M1	d						
		M2	d						
		M3	d						
		M4	d,e	e	e	e	e	e	e
		M5	d						
4007 CMOS	C	M1							
		M2							
		M3							
		M4							
		M5							
741 Linear	E	M1							
		M2							
		M3							
		M4							
		M5							

Series a

The following sequence of histograms shows the variations in V_{OL}, V_{OH}, and V_{IC} for Manufacturer D 5400 TTL Group 201 parts measured at +25°C as a function of the following environments (see Figure 4-1).

Measurement	Preceding Environment
M1	Initial measurement
M2	15 cycles thermal shock -65°C to +150°C
M3	Moisture resistance, 10 @ 98%RH 25°C to 65°C
M4	1000 hours operating life at +5°C
M5	1000 hours operating life at +125°C

For V_{OL}, there were measurements made on each of the four outputs of each part. These measurements are all combined in the distribution histogram, to give a total of 200 measurements on the 50 parts in the group.

For V_{OH}, there were two measurements made on each of four outputs for a total of 8 V_{OH} measurements per part. These are all combined to give a total of 400 measurements on the 50 parts in the group.

For V_{IC}, there were measurements made on each of the eight inputs of each part. These measurements were also combined in the distribution histogram to give 400 measurement on the 50 parts in the group.

Table B-2. Series a Histograms

Part Type	Mfr.	Measurement	201	202	203	204	205	206	207
7400 TTL	A	M1							
		M2							
		M3							
		M4							
		M5							
5400 TTL	B	M1							
		M2							
		M3							
		M4							
		M5							
5400 TTL	C	M1							
		M2							
		M3							
		M4							
		M5							
7400 TTL	D	M1	a						
		M2	a						
		M3	a						
		M4	a						
		M5	a						
4007 CMOS	E	M1							
		M2							
		M3							
		M4							
		M5							
4007 CMOS	C	M1							
		M2							
		M3							
		M4							
		M5							
741 Linear	E	M1							
		M2							
		M3							
		M4							
		M5							

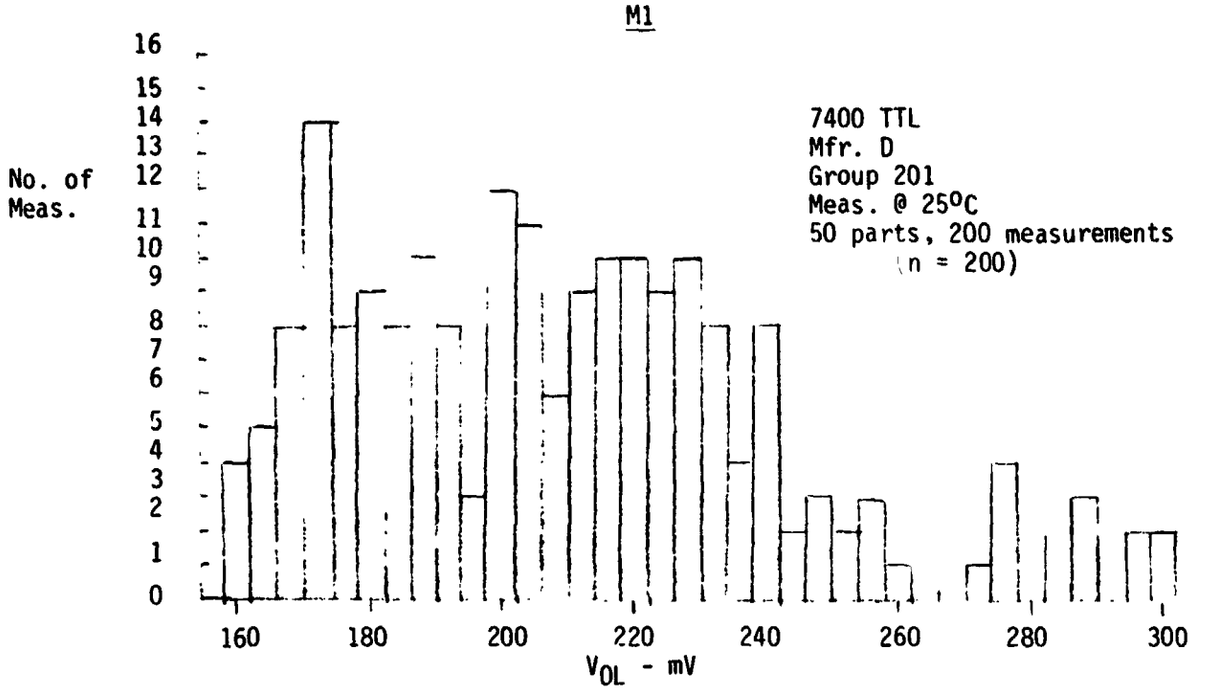


Figure B-1 Initial Distribution of V_{OL1}

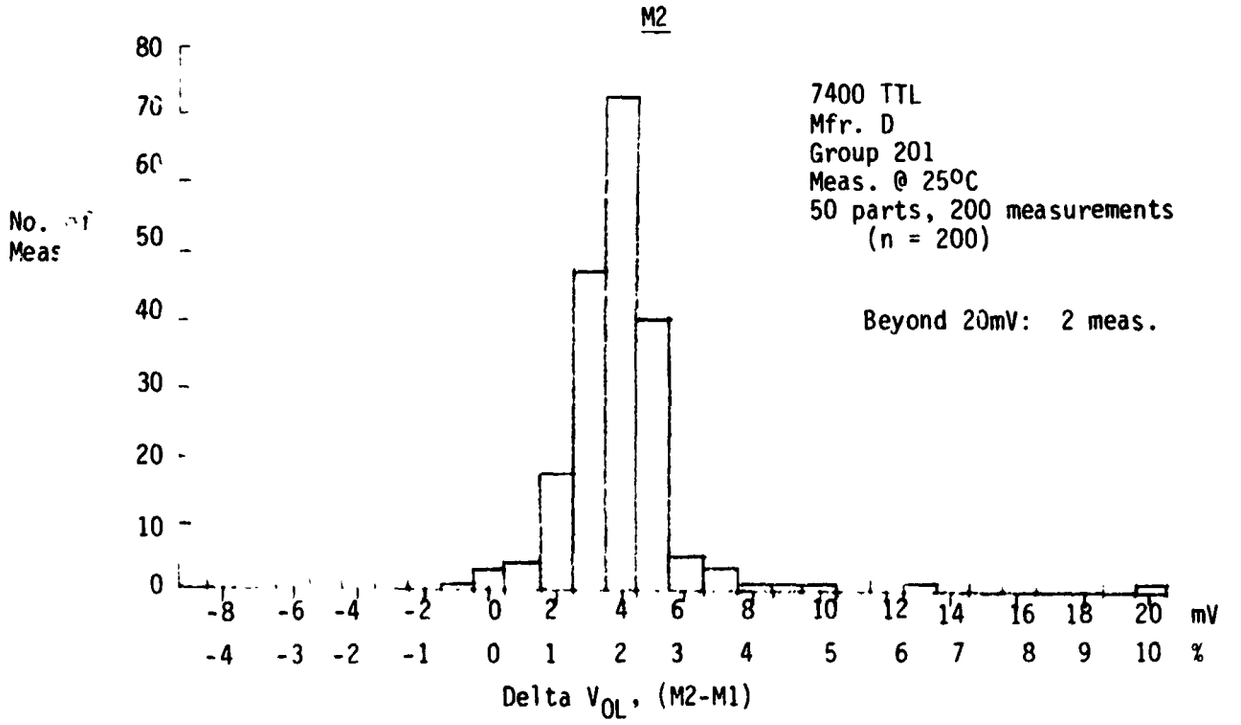


Figure B-2 Distribution of Delta V_{OL} After Thermal Shock

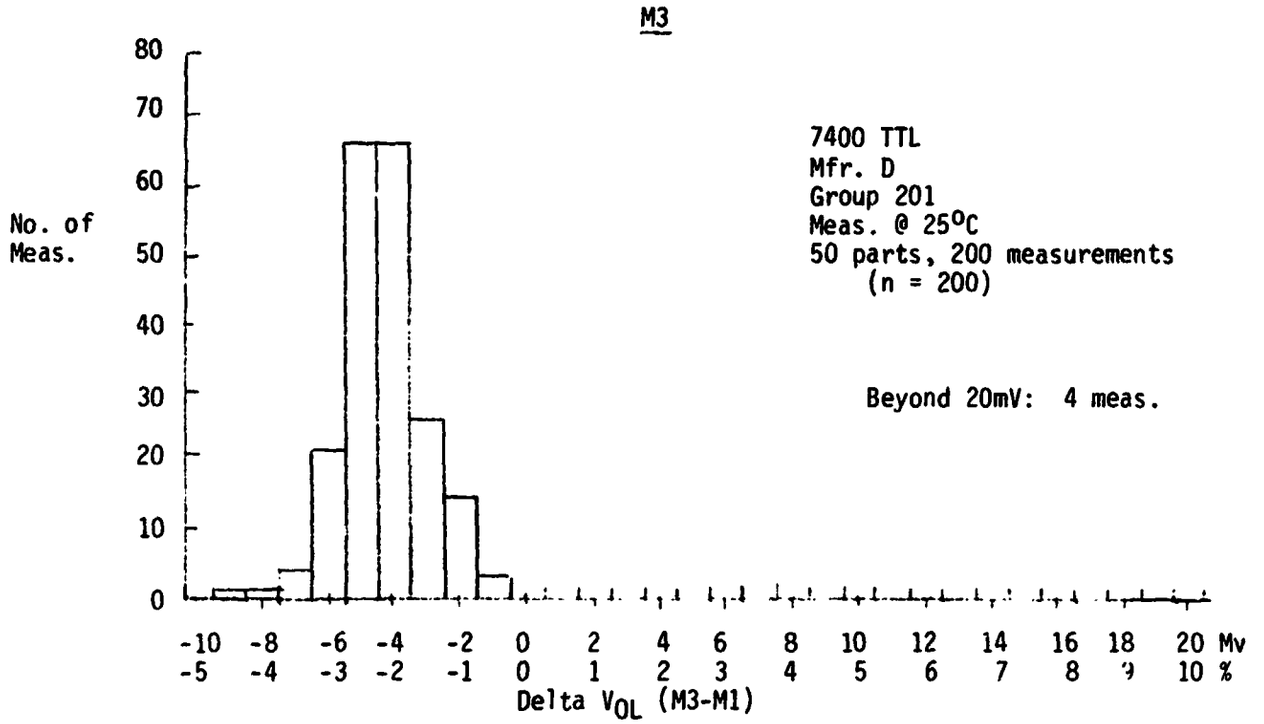


Figure B-3 Distribution of Delta V_{OL} After Moisture Resistance

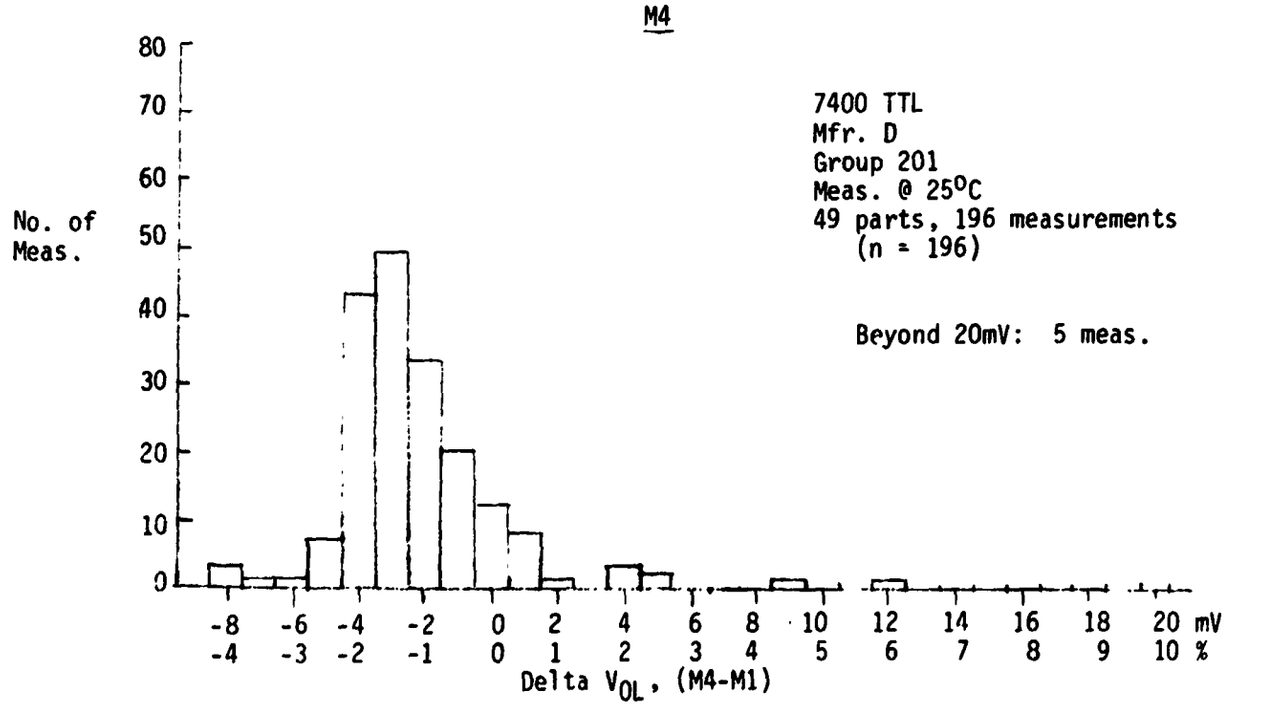


Figure B-4 Distribution of Delta V_{OL} After Low Temp. Life

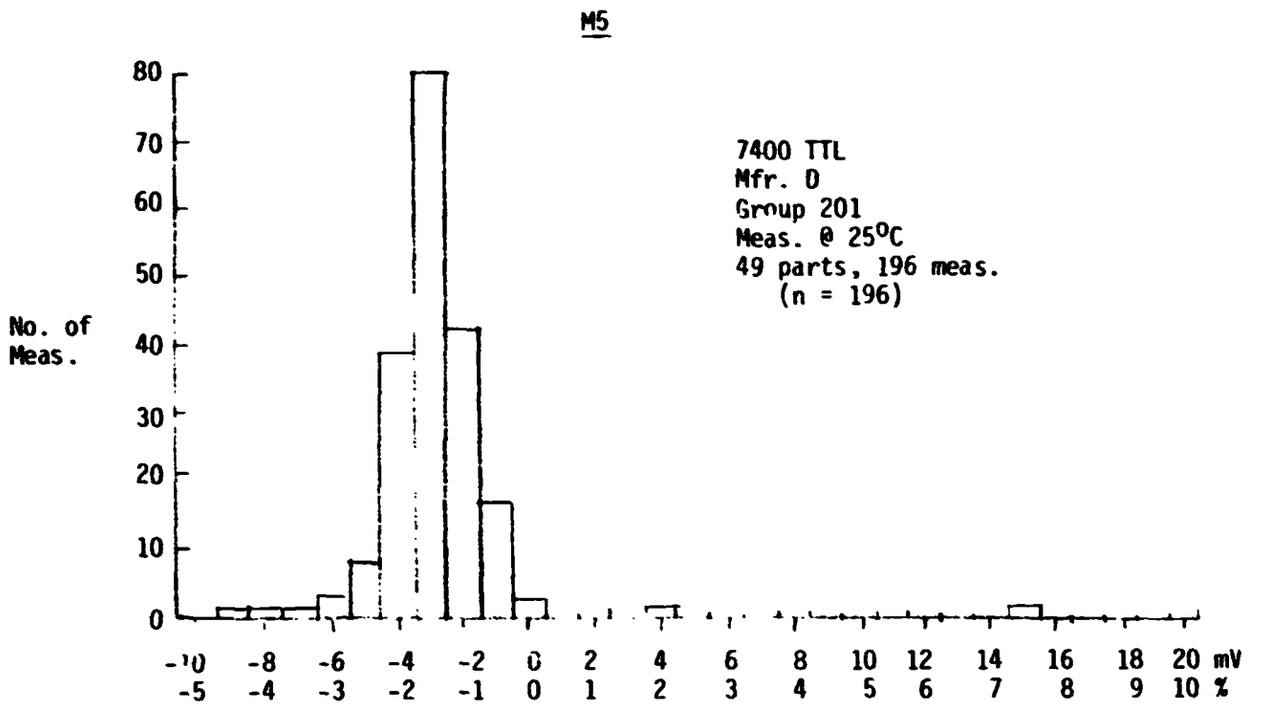


Figure B-5. Distribution of Delta V_{OL} After Hi Temp Life

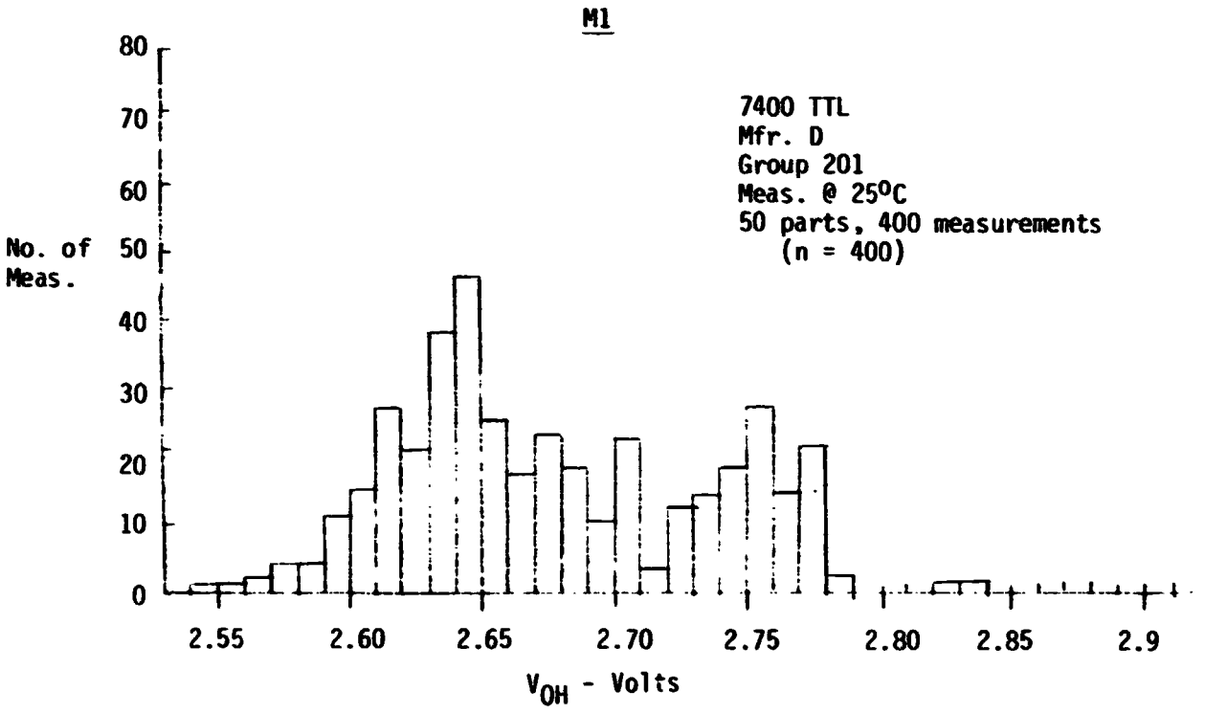


Figure B-6. Initial Distribution of V_{OH}

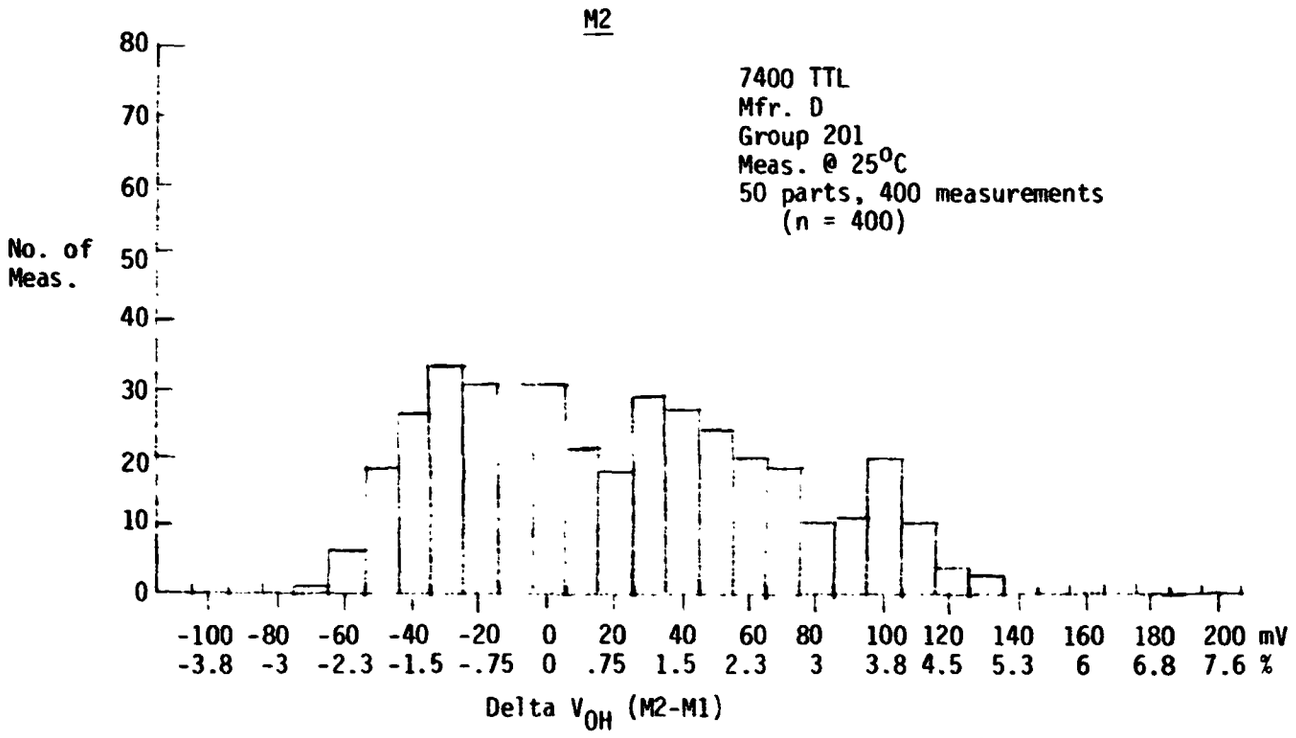


Figure B-7. Distribution of Delta V_{OH} After Thermal Shock

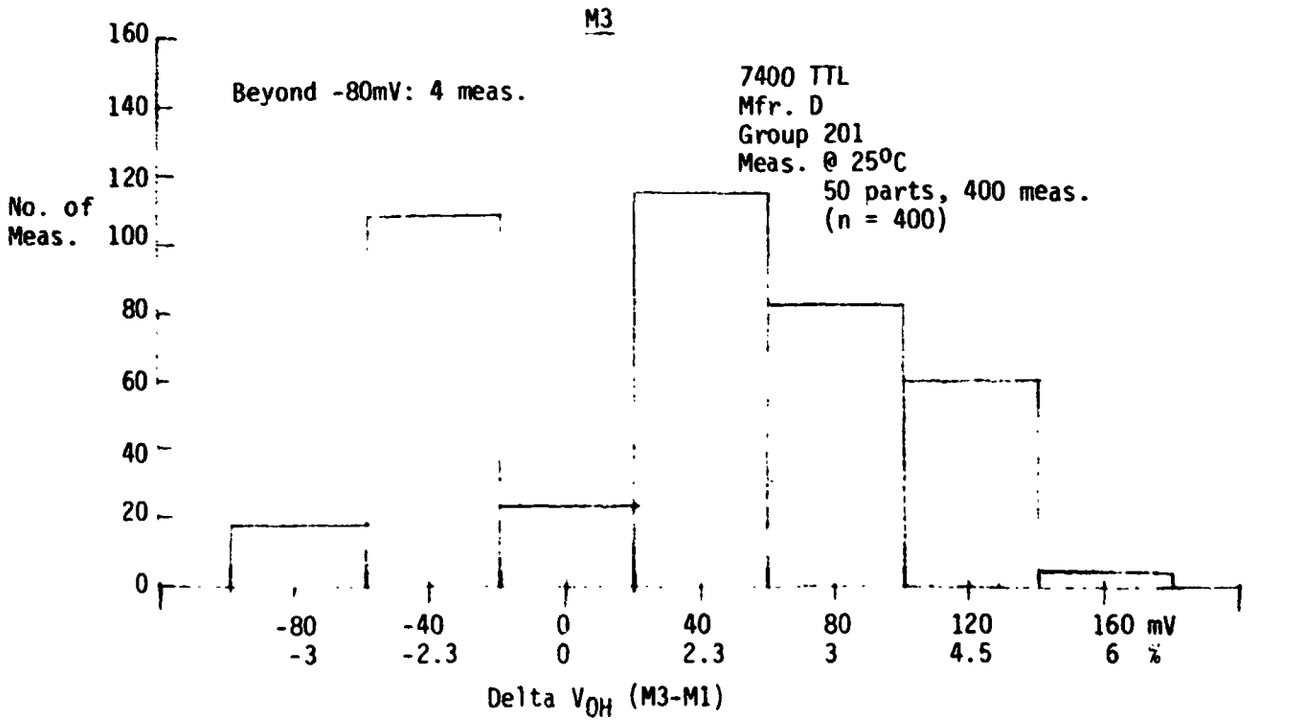


Figure B-8. Distribution of Delta V_{OH} After Moisture Resistance

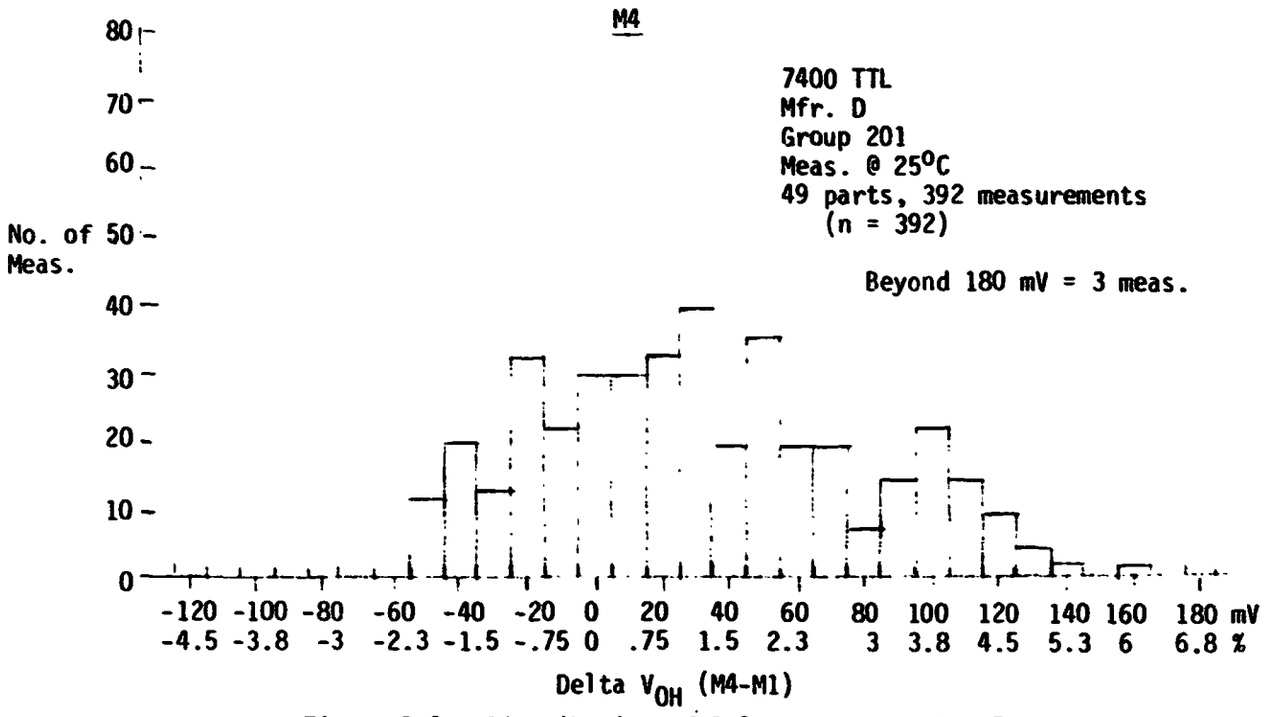


Figure B-9. Distribution of Delta V_{OH} After Low Temp Life

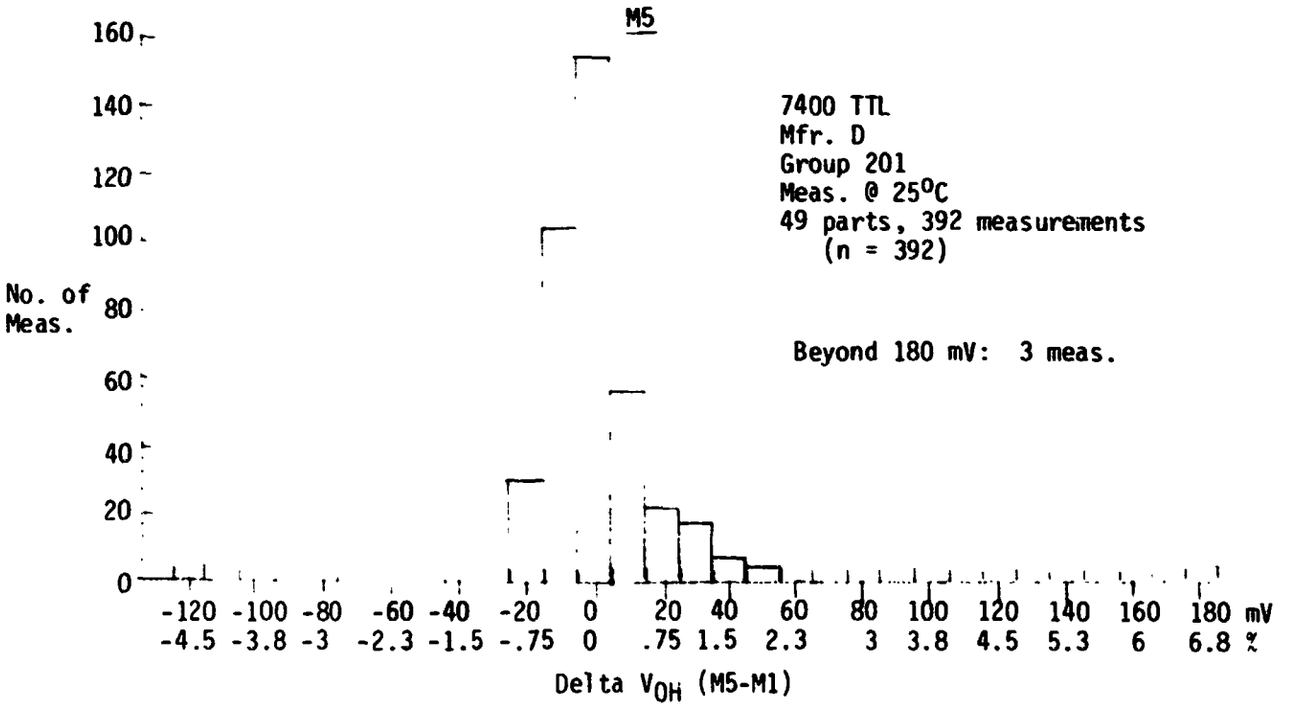


Figure B-10. Distribution of Delta V_{OH} After Hi Temp Life

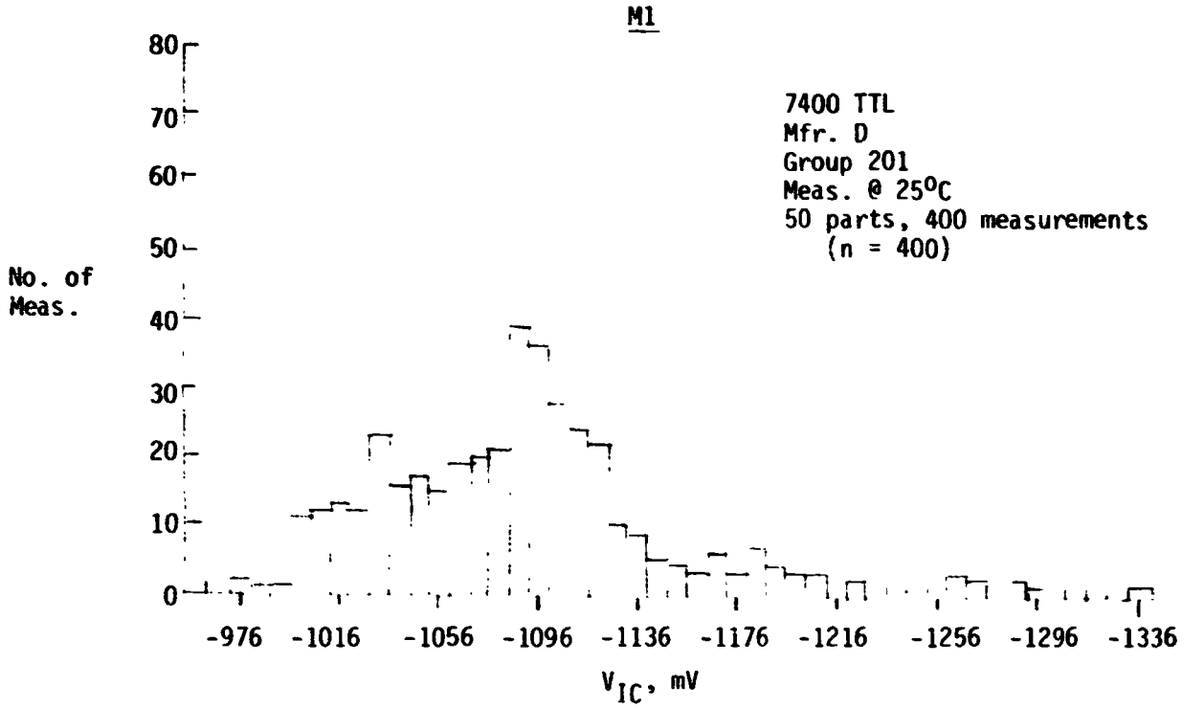


Figure B-11. Initial Distribution of V_{IC}

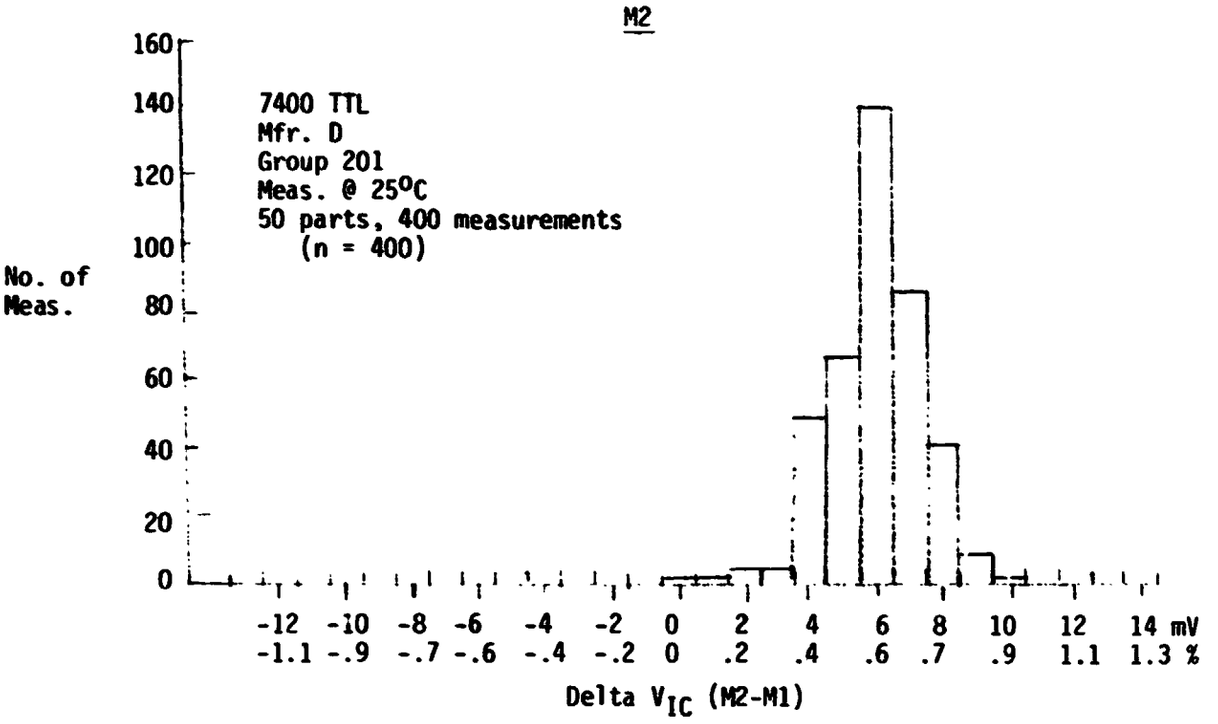


Figure B-12. Distribution of Delta V_{IC} After Thermal Shock

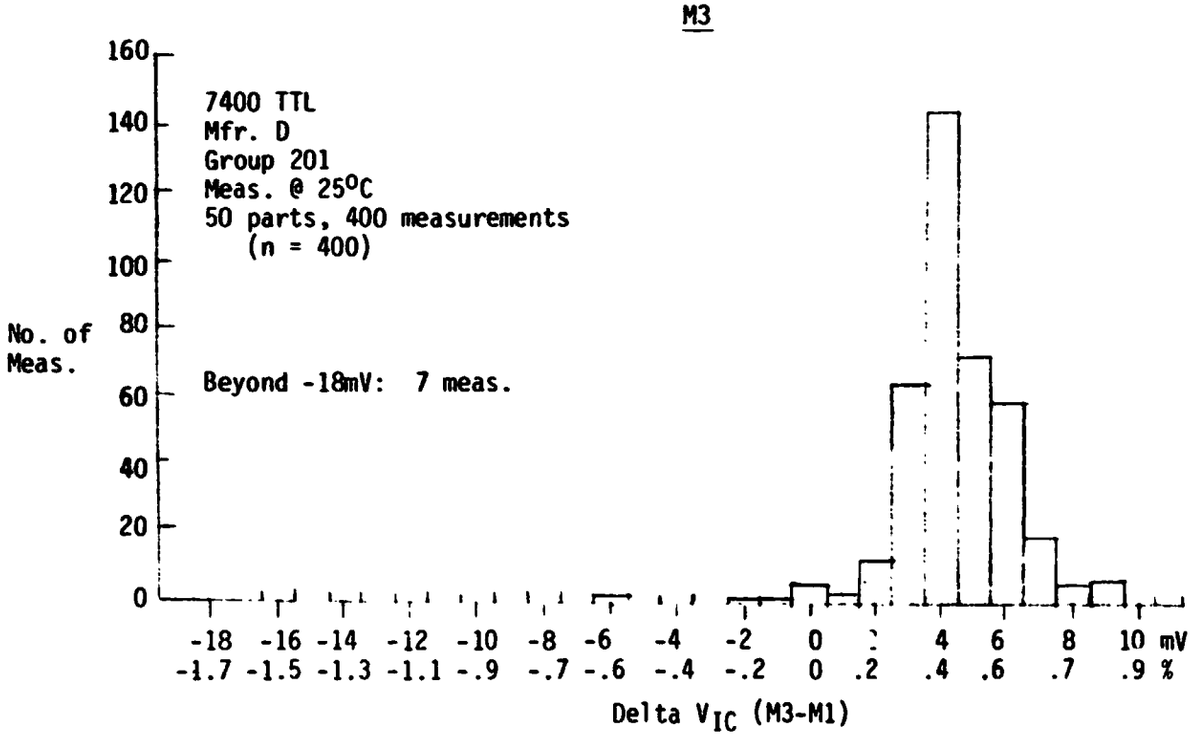


Figure B-13. Distribution of Delta V_{IC} After Moisture Resistance

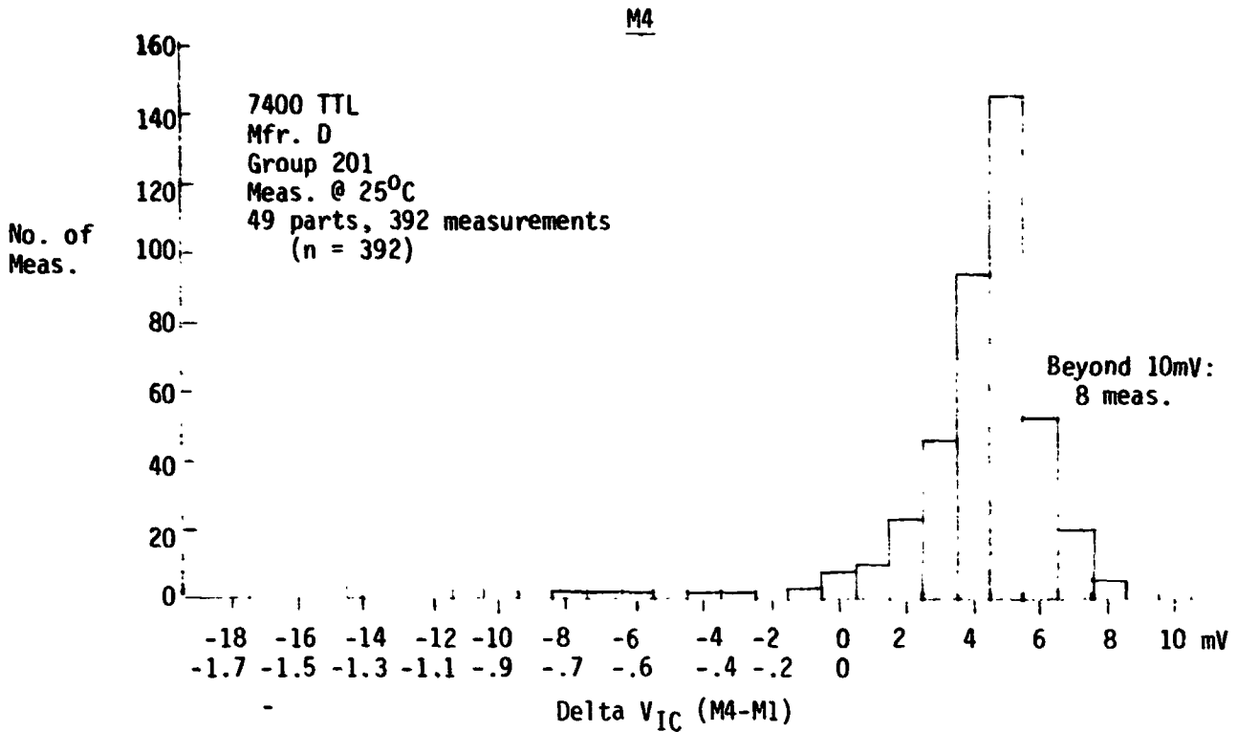


Figure B-14. Distribution of Delta V_{IC} After Low Temp Life

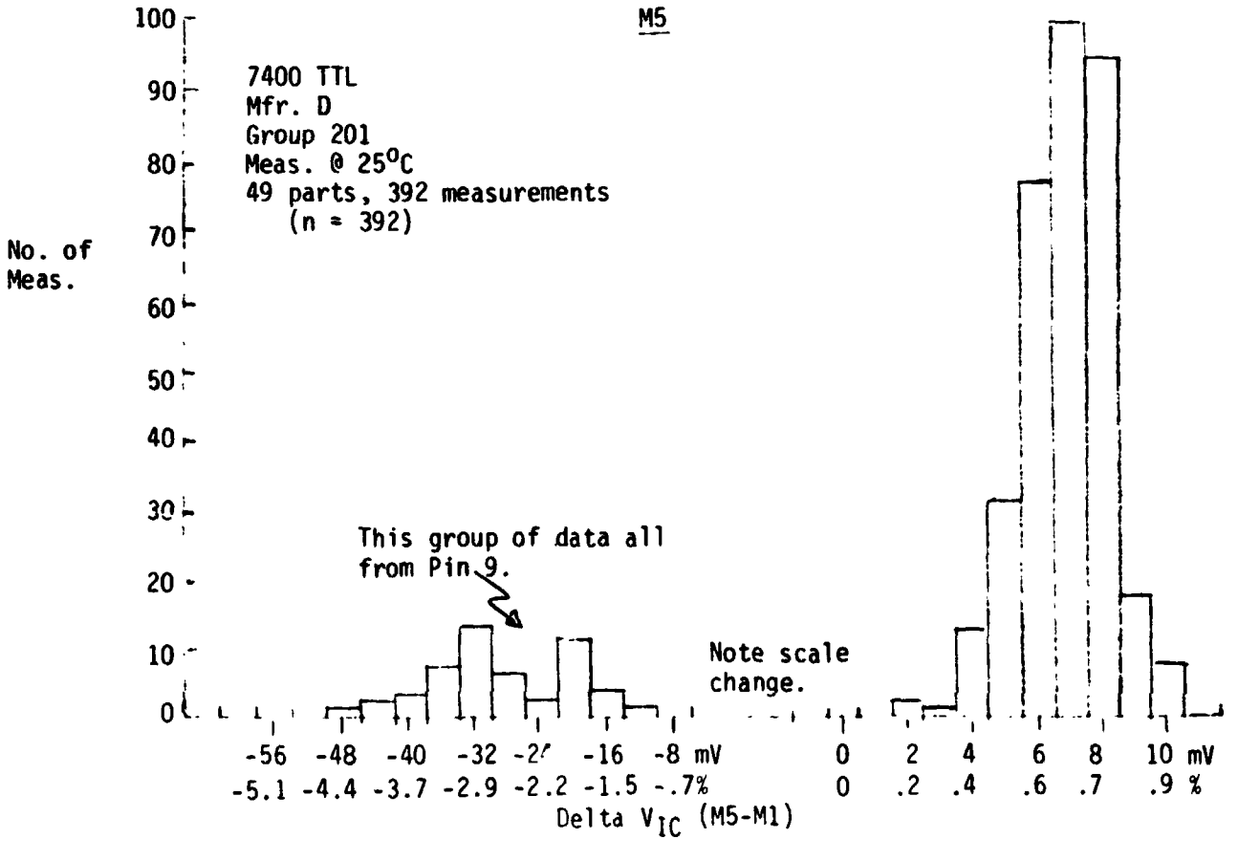


Figure B-15. Distribution of Delta V_{IC} After Hi Temp Life

Series b

The following sequence of distribution histograms presents the variations in V_{OH}, V_{OL}, and V_{IC} for the Manufacturer D 7400 TTL devices in environmental stress groups 202 through 207. The data at M4 is presented.

Again all measurements are combined into composite histograms: 4 V_{OL}s, 8 V_{OH}s, and 8 V_{IC}s per part.

For the corresponding Group 201 distribution, see Figures B-4 (Delta V_{OL}), B-9 (Delta V_{OH}), and B-14 (Delta V_{IC}).

For a complete definition of the prior environments experienced by each group, refer to Figure 3-4.

Table B-3. Series b Histograms

Part Type	Mfr.	Measurement	201	202	203	204	205	206	207
7400 TTL	A	M1							
		M2							
		M3							
		M4							
		M5							
5400 TTL	B	M1							
		M2							
		M3							
		M4							
		M5							
5400 TTL	C	M1							
		M2							
		M3							
		M4							
		M5							
7400 TTL	D	M1							
		M2							
		M3							
		M4	b*	b	b	b	b	b	b
		M5							
4007 CMOS	E	M1							
		M2							
		M3							
		M4							
		M5							
4007 CMOS	C	M1							
		M2							
		M3							
		M4							
		M5							
741 Linear	E	M1							
		M2							
		M3							
		M4							
		M5							

*See Figures B-4, B-9, and B-14.

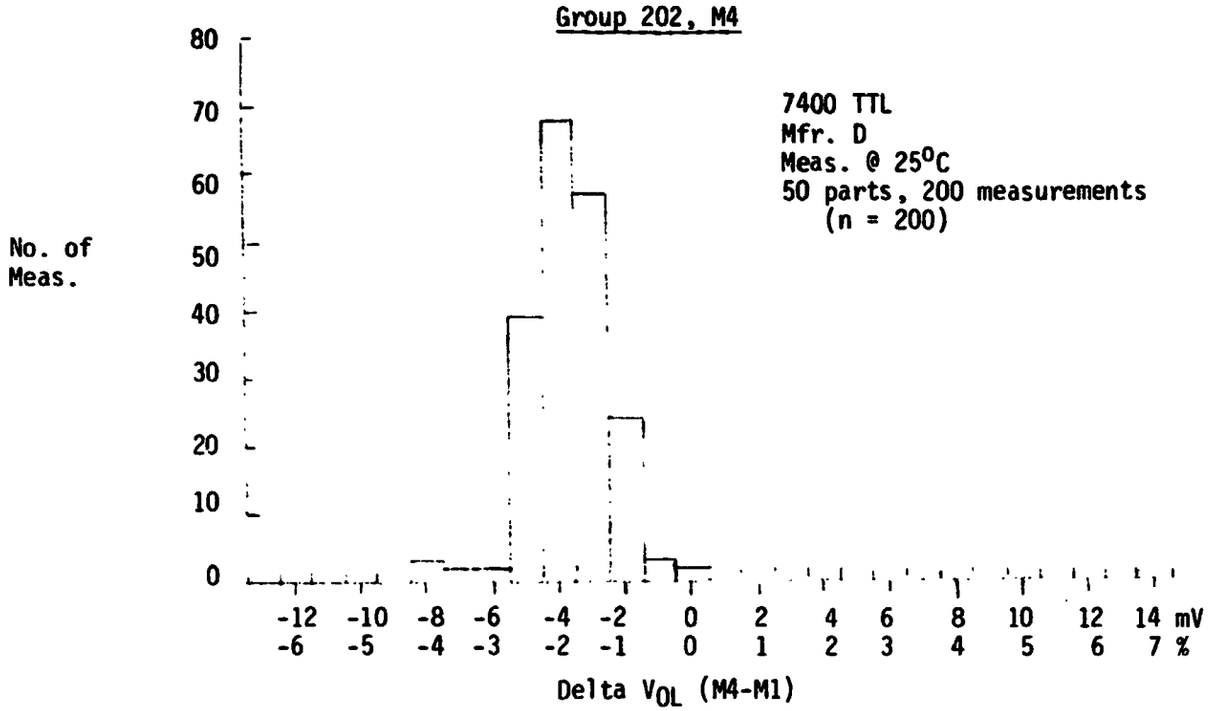


Figure B-16. Distribution of Delta V_{OL} After 4000 Temp Cycles

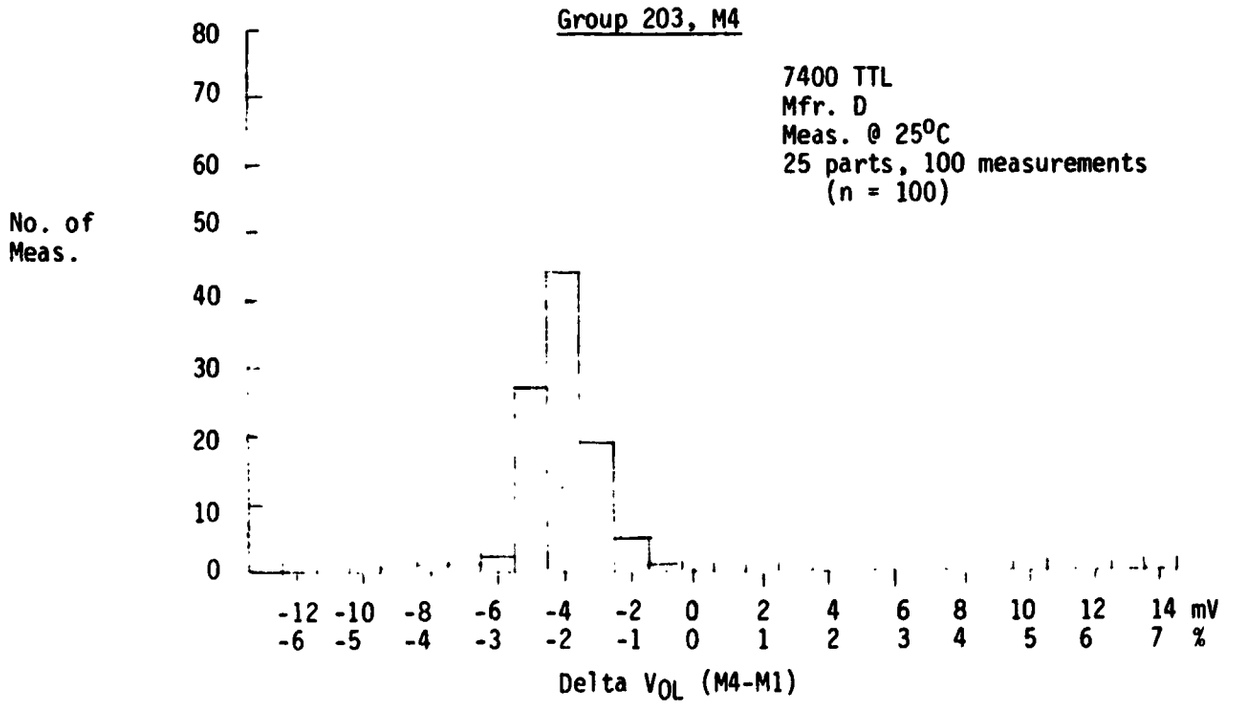


Figure B-17. Distribution of Delta V_{OL} After 70g Vibration

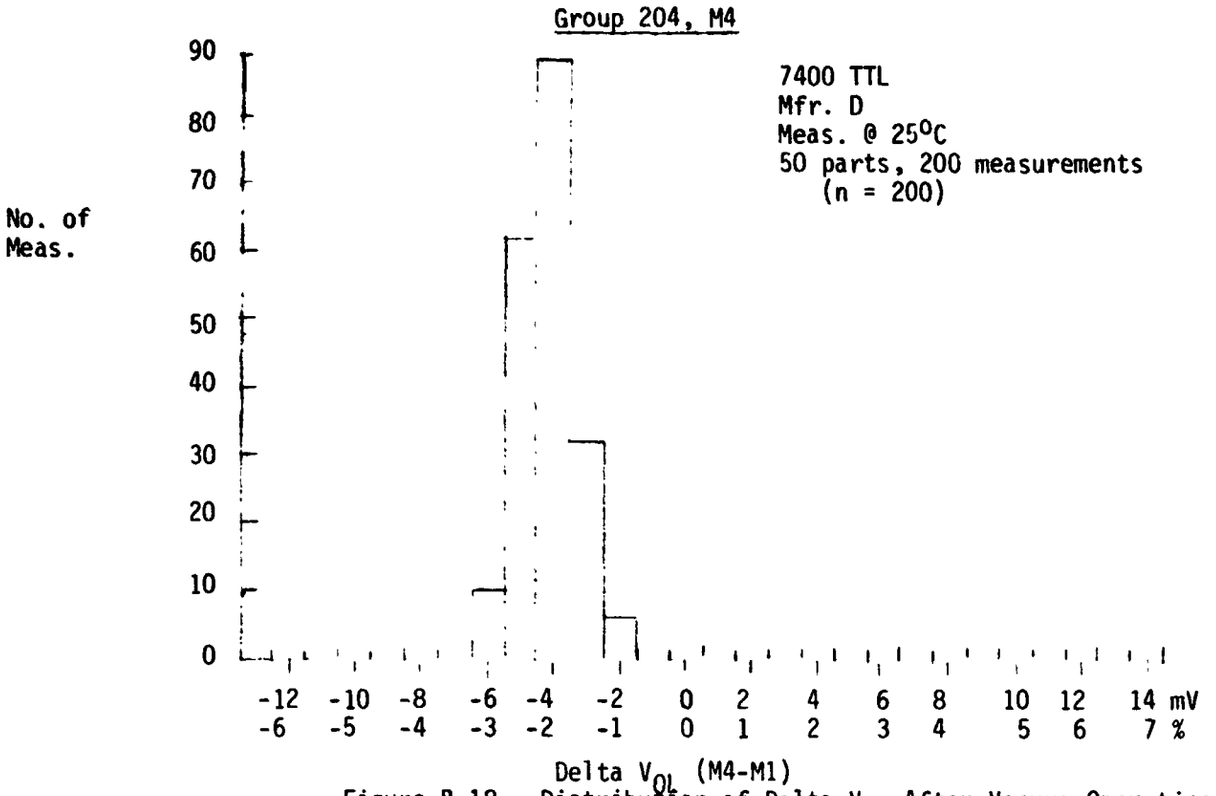


Figure B-18. Distribution of Delta V_{OL} After Vacuum Operating Life

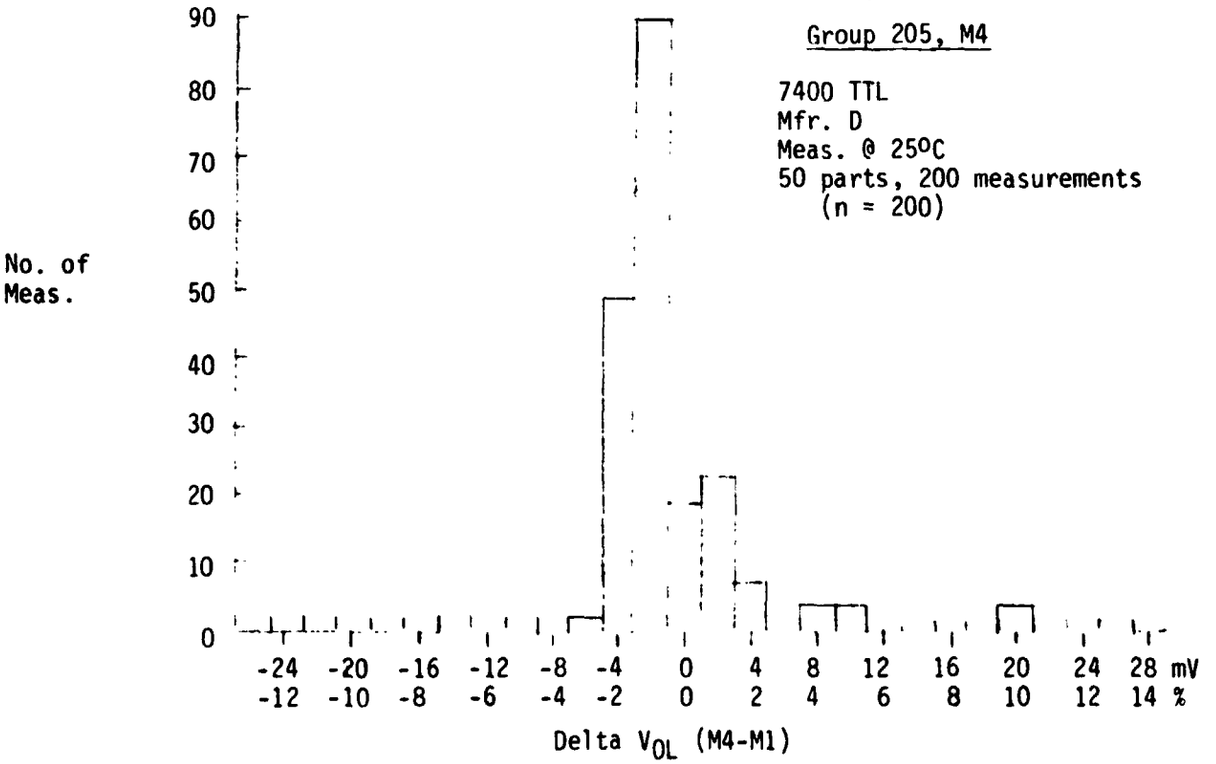


Figure B-19. Distribution of V_{OL} After Low Temp Operating Life

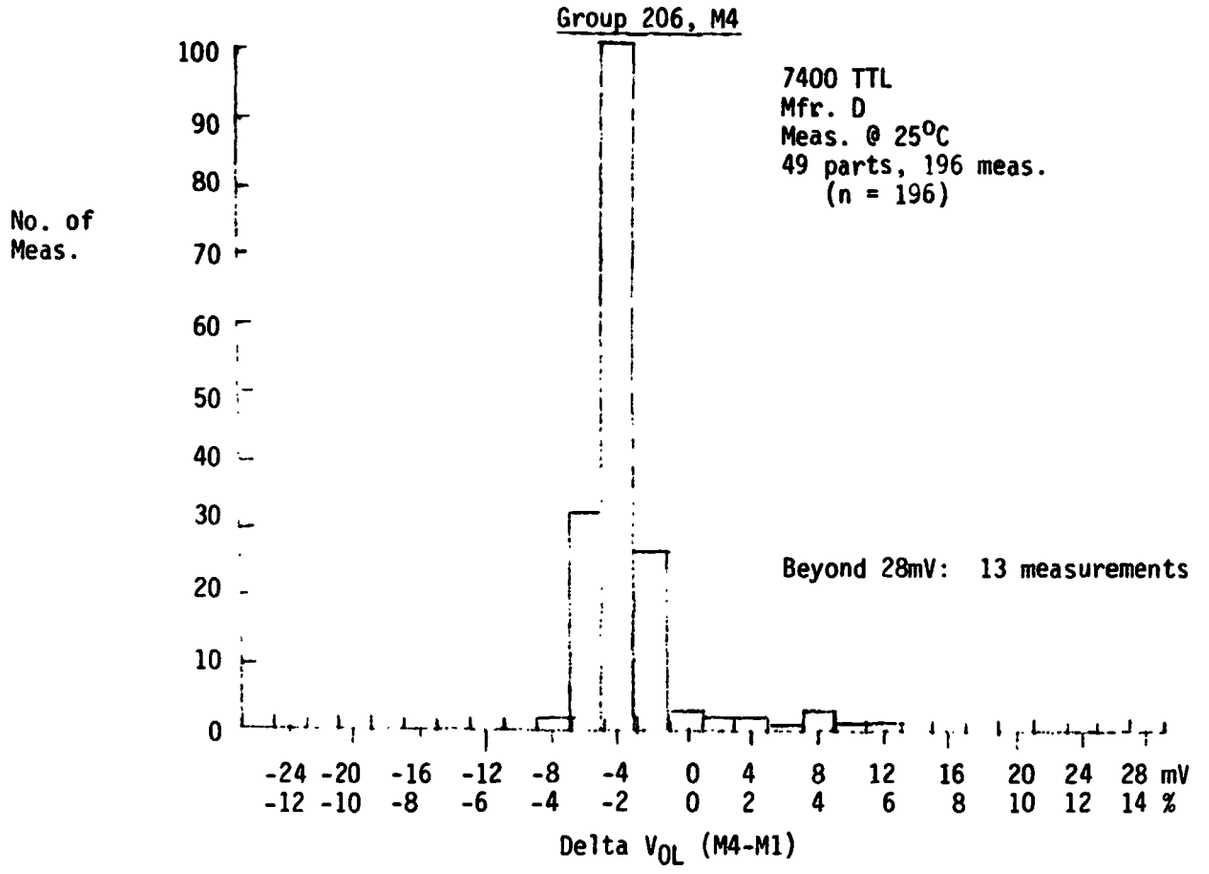


Figure B-20. Distribution of Delta V_{OL} After Hi Temp Life

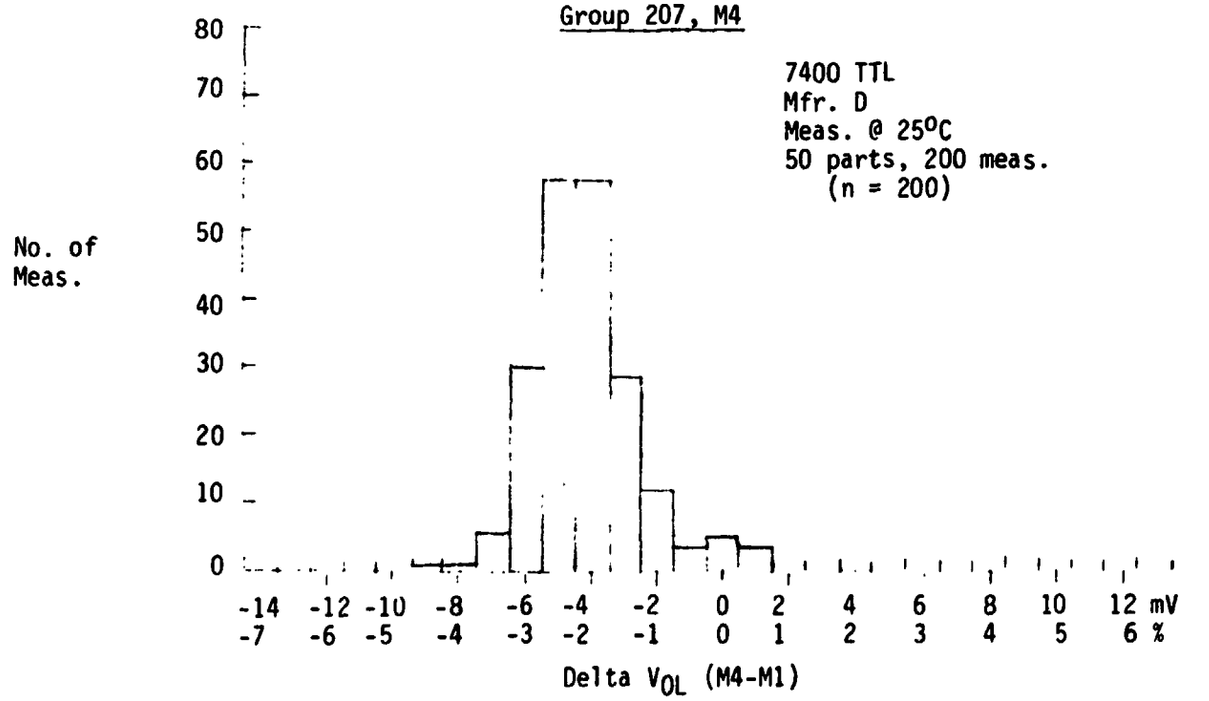


Figure B-21. Distribution of Delta V_{OL} After Low Temp Life

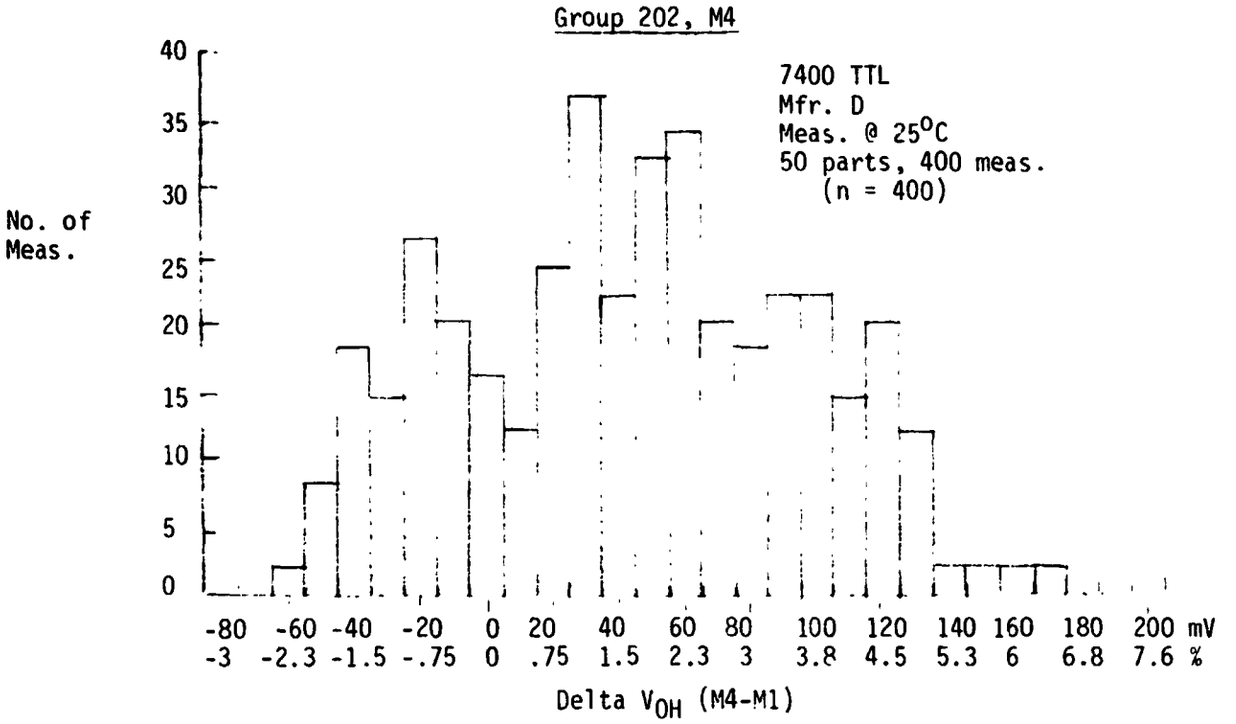


Figure B-22. Distribution of Delta V_{OH} After Low Temp Life

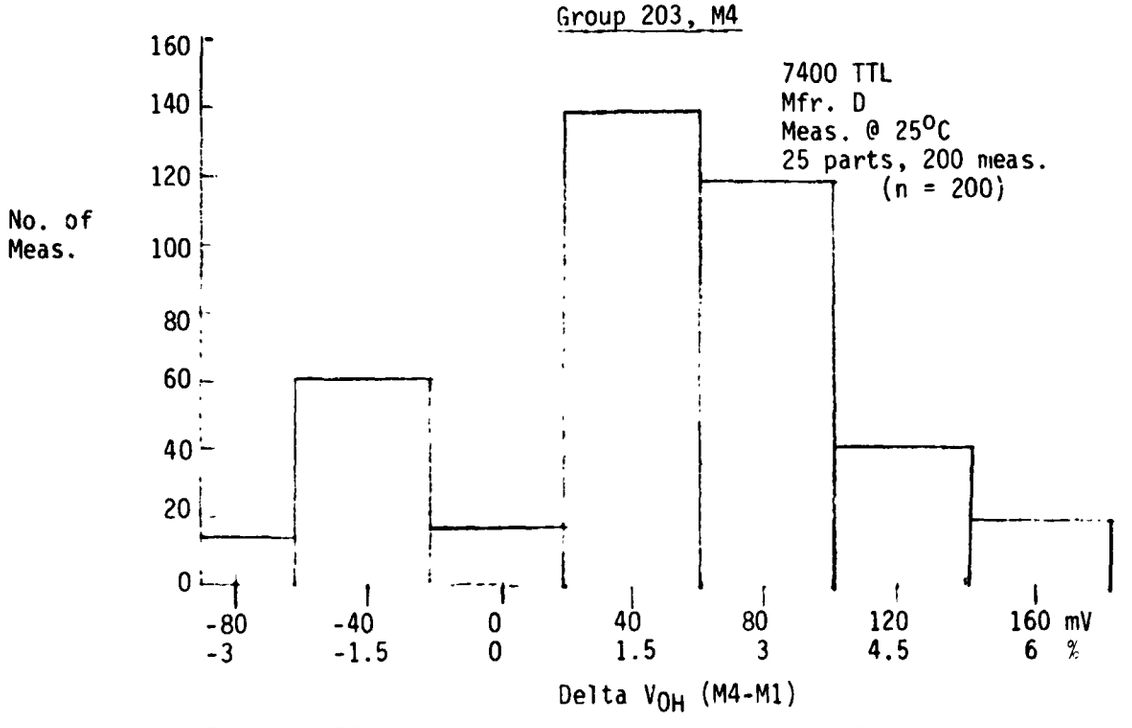


Figure B-23. Distribution of Delta V_{OH} After 70g Vibration

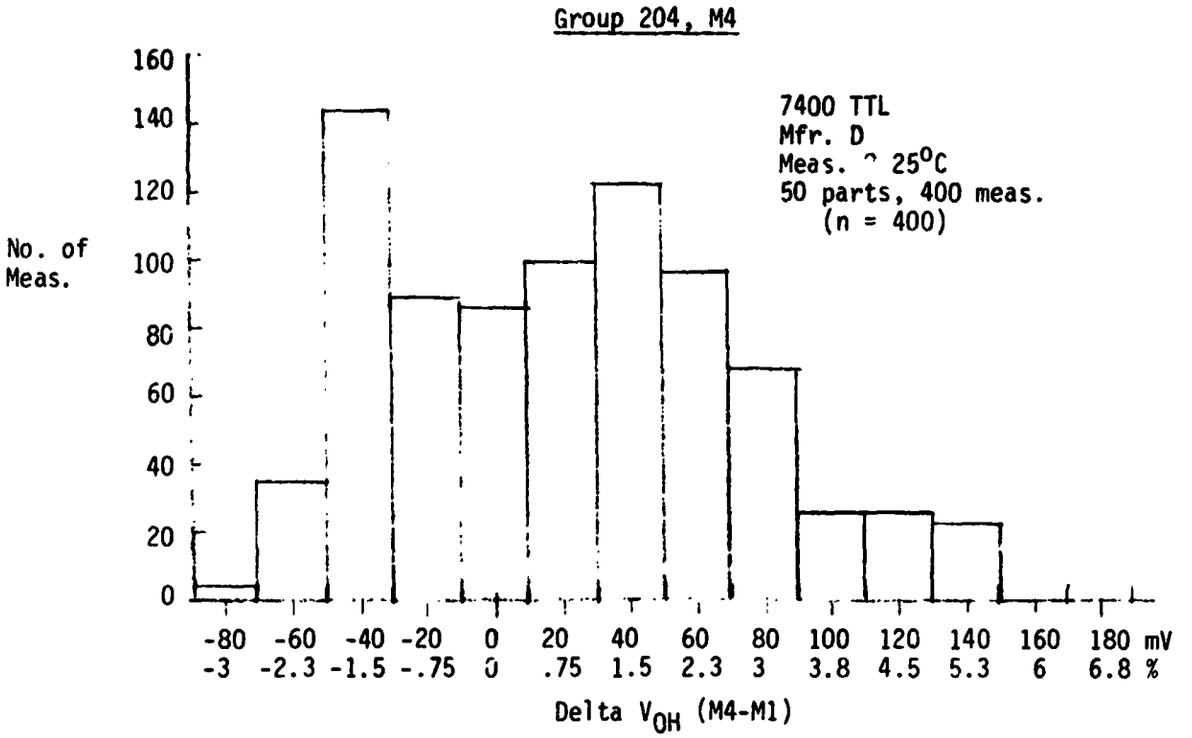


Figure B-24. Distribution of Delta V_{OH} After Vacuum Life

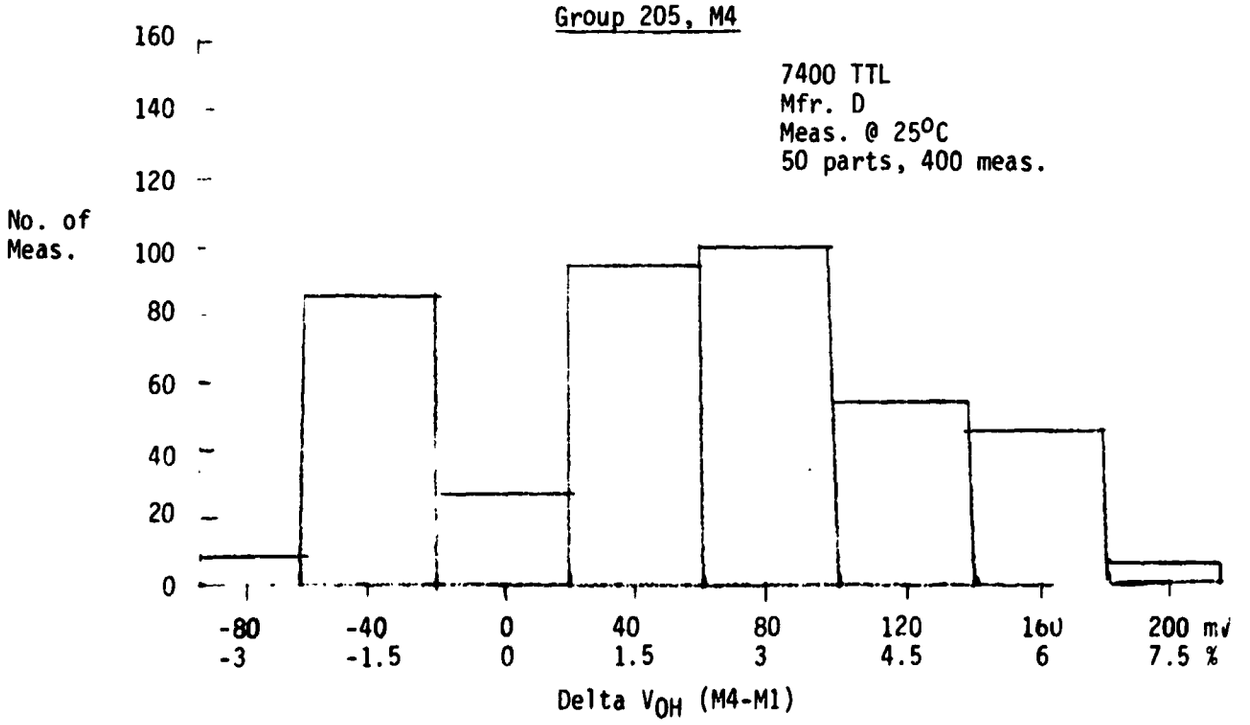


Figure B-25. Distribution of Delta V_{OH} After Low Temp Life

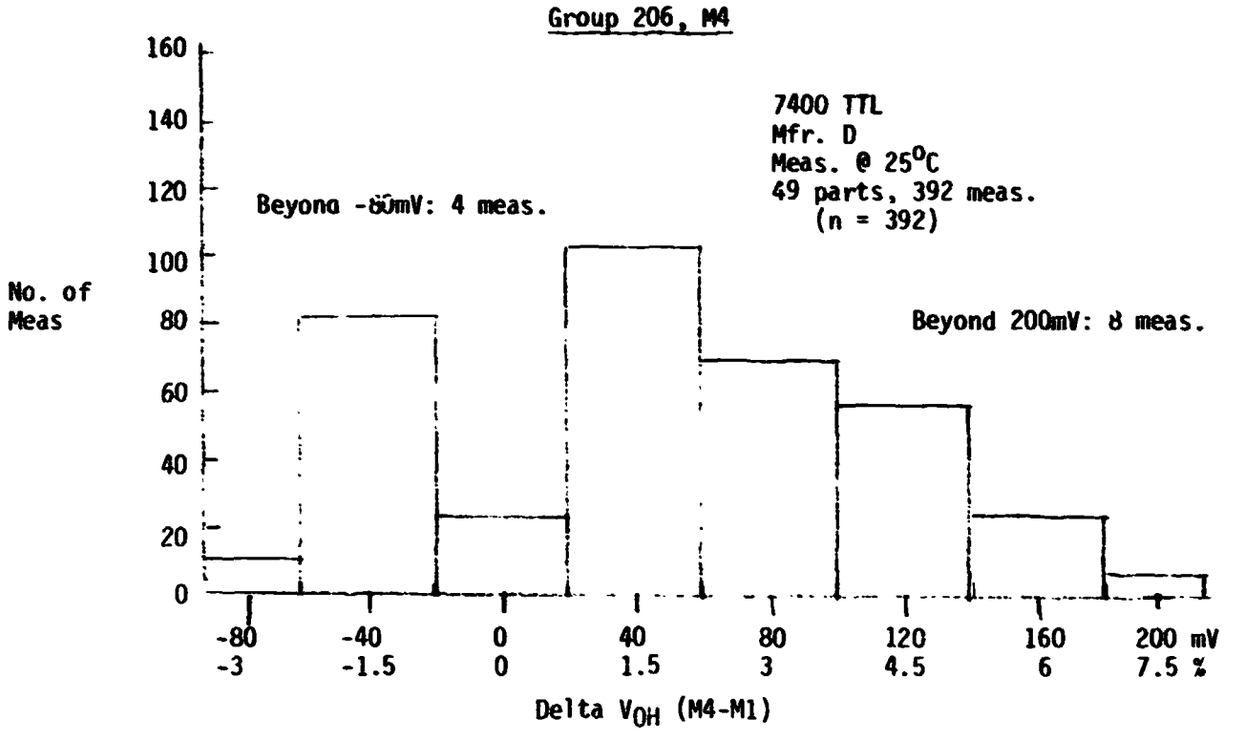


Figure B-26. Distribution of Delta V_{OH} After Hi Temp Life

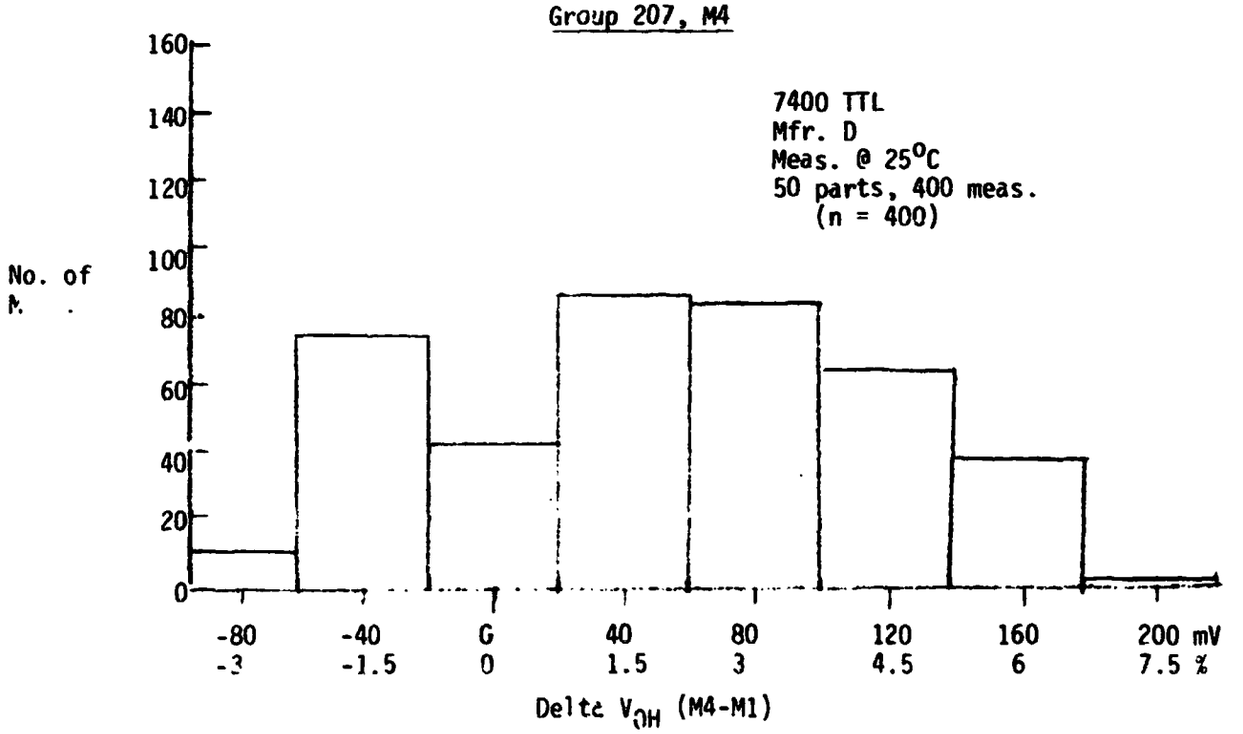


Figure B-27. Distribution of Delta V_{OH} After Low Temp Life

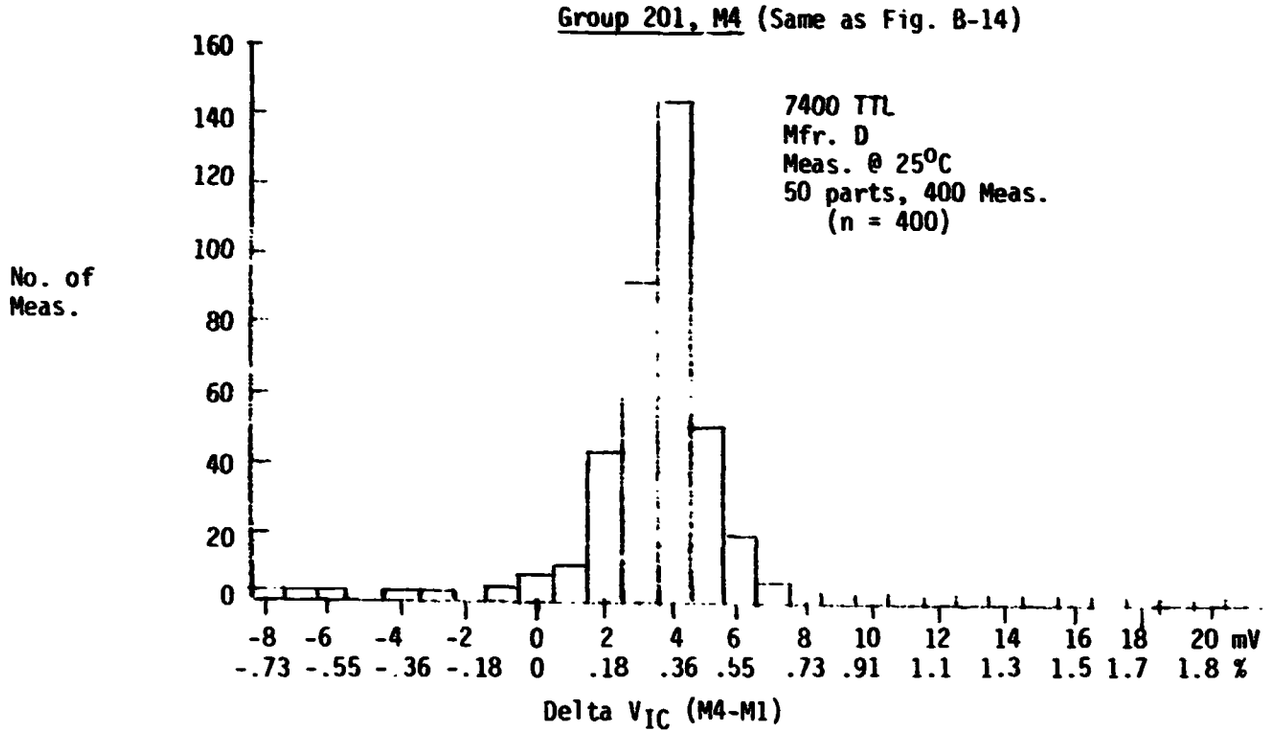


Figure B-28. Distribution of Delta V_{IC} After Low Temp Life

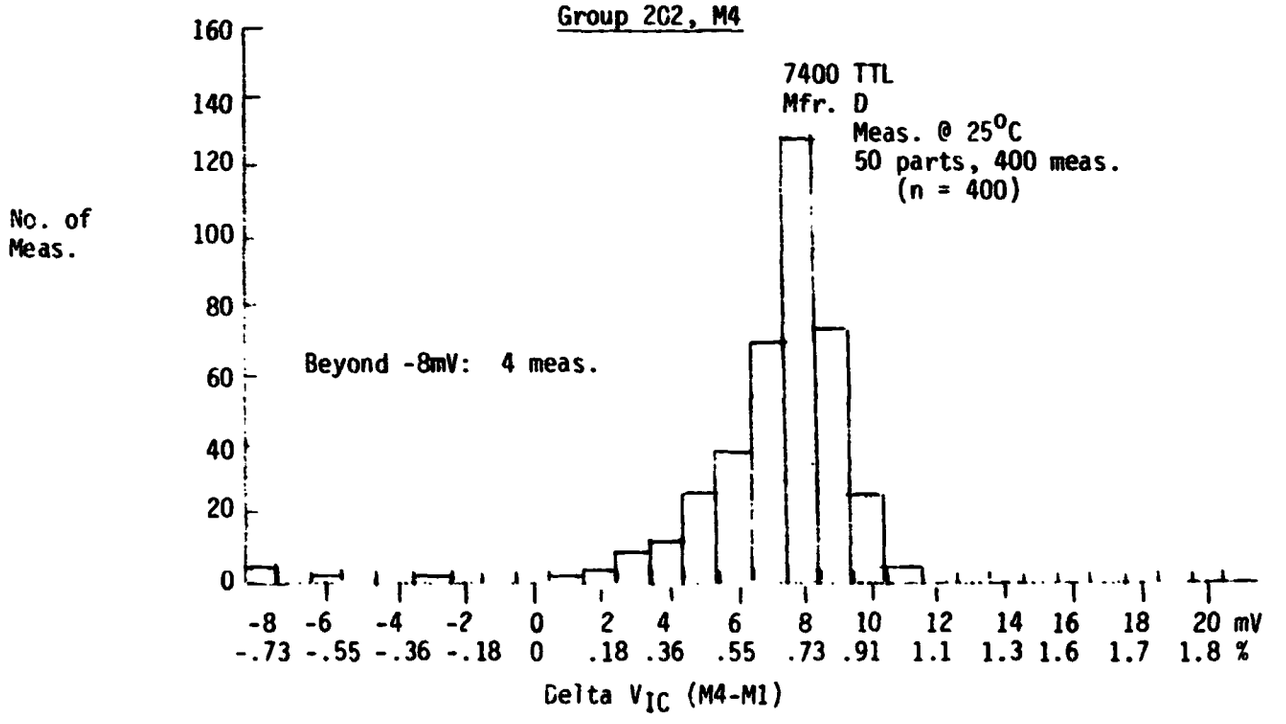


Figure B-29. Distribution of Delta V_{IC} After 4000 Temp Cycles

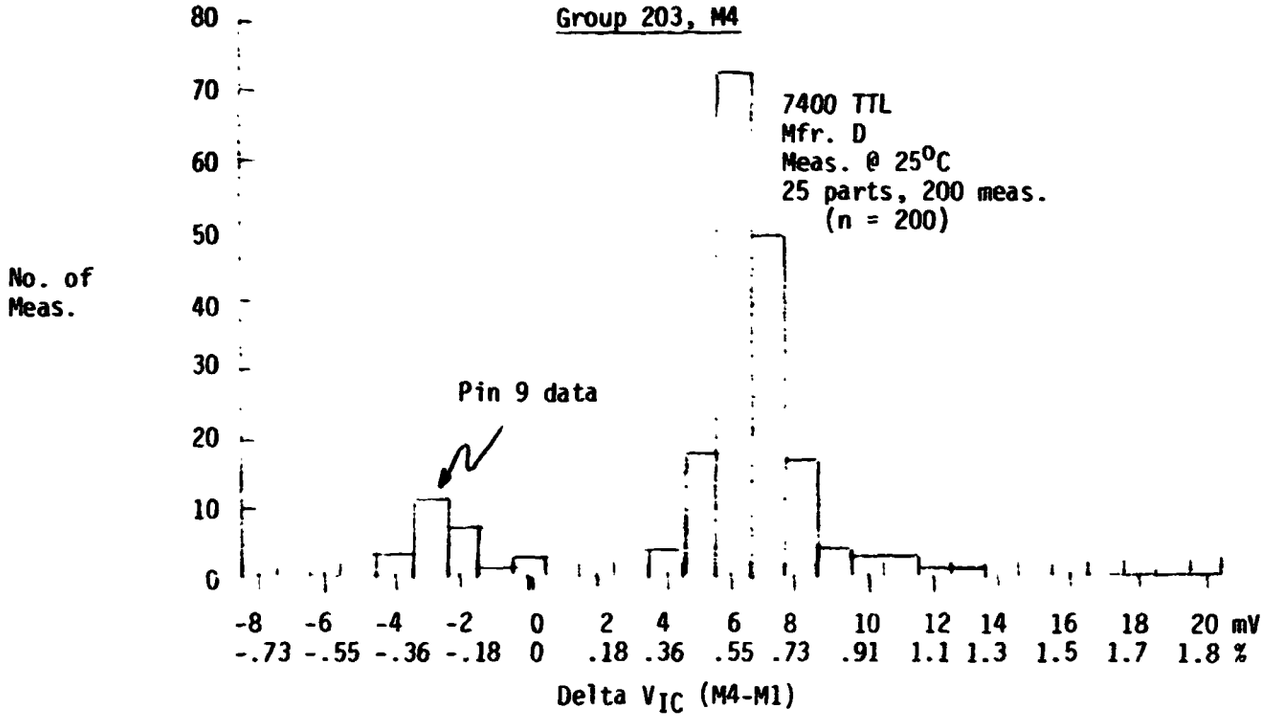


Figure B-30. Distribution of Delta V_{IC} After 70g Vibration

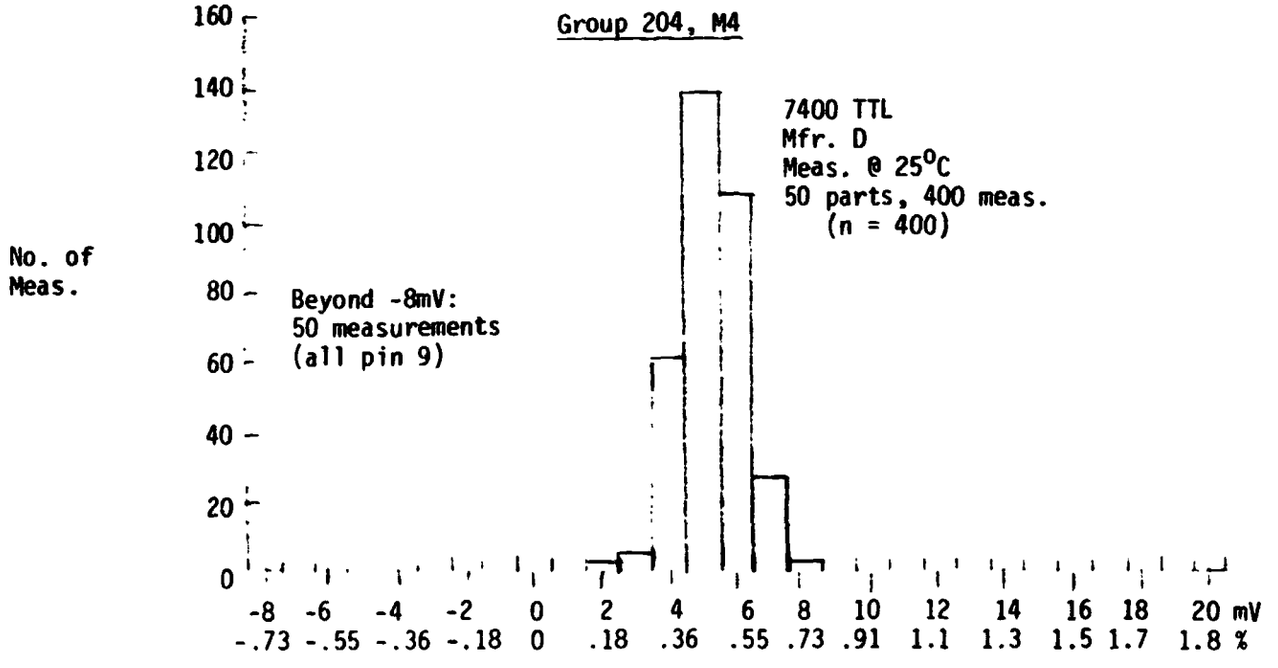


Figure B-31. Distribution of Delta V_{IC} After Vacuum Life

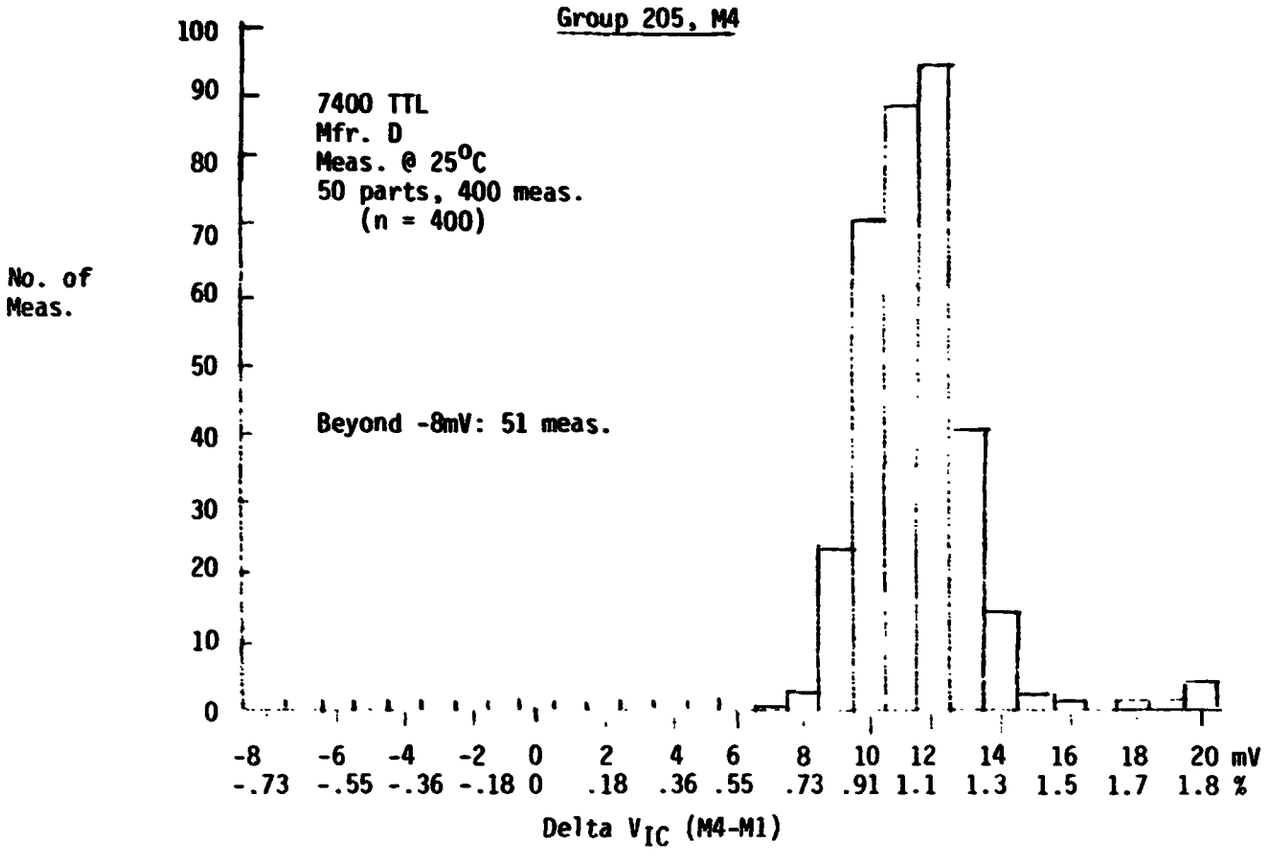


Figure B-32. Distribution of Delta V_{IC} After Low Temp Life

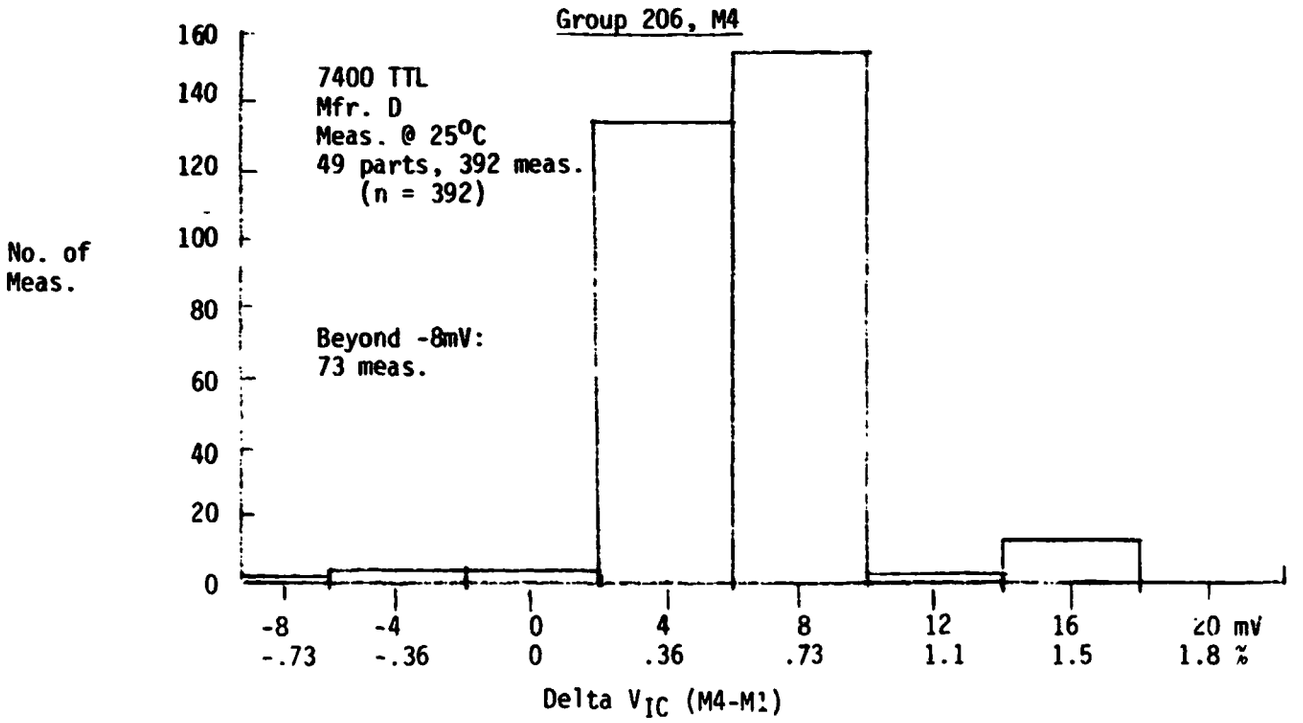


Figure B-33. Distribution of Delta V_{IC} After Hi Temp Life

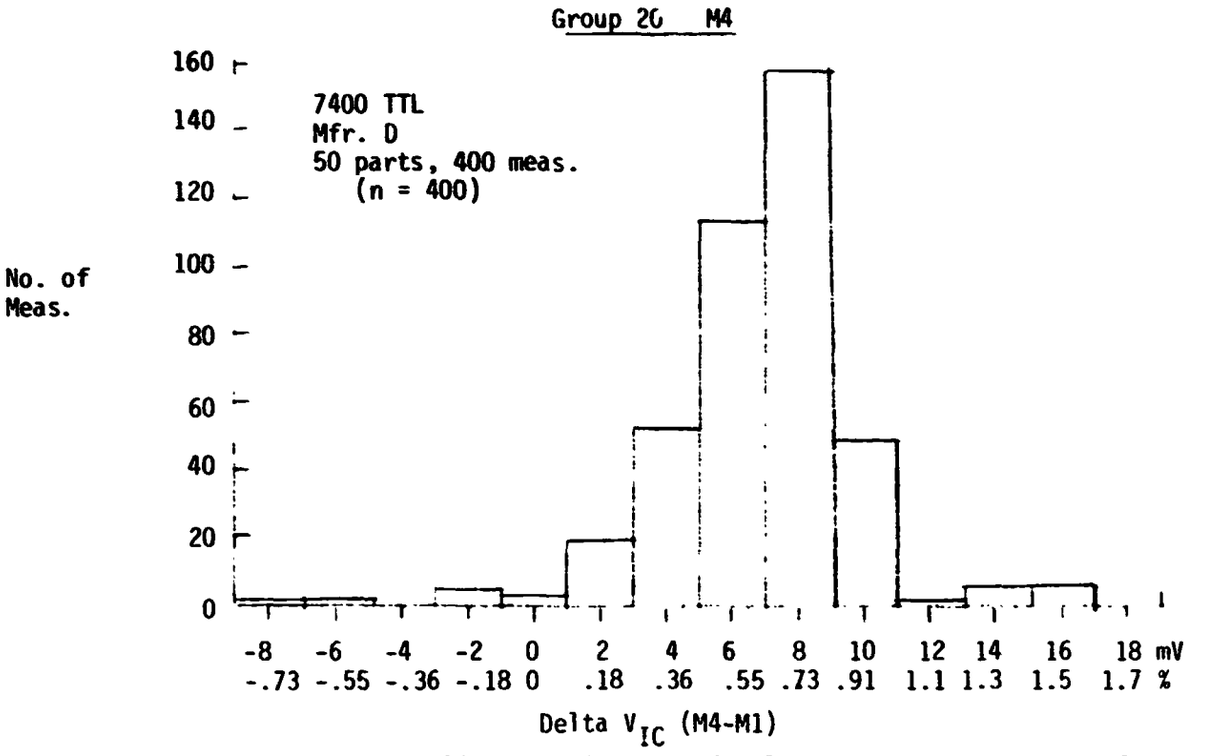


Figure B-34. Distribution of Delta V_{IC} After Low Temp Life

Series c

The following sequence of histograms shows the variations in V_{OL} at M2 and M3 of Group 201 for the other three TTL manufacturers not previously treated: Manufacturer A 7400 TTL and Manufacturers B and C 5400 TTL. Again the four V_{OL} measurements made on each part are all combined to give a total of 200 measurements for the 50 parts in each group.

Table B-4. Series c Histograms

Part Type	Mfr.	Measurement	201	202	203	204	205	206	207
7400 TTL	A	M1							
		M2	c						
		M3	c						
		M4							
		M5							
5400 TTL	B	M1							
		M2	c						
		M3	c						
		M4							
		M5							
5400 TTL	C	M1							
		M2	c						
		M3	c						
		M4							
		M5							
7400 TTL	D	M1							
		M2	c (Figure B-2)						
		M3	c (Figure B-3)						
		M4							
		M5							
4007 CMOS	E	M1							
		M2							
		M3							
		M4							
		M5							
4007 CMOS	C	M1							
		M2							
		M3							
		M4							
		M5							
741 Linear	E	M1							
		M2							
		M3							
		M4							
		M5							

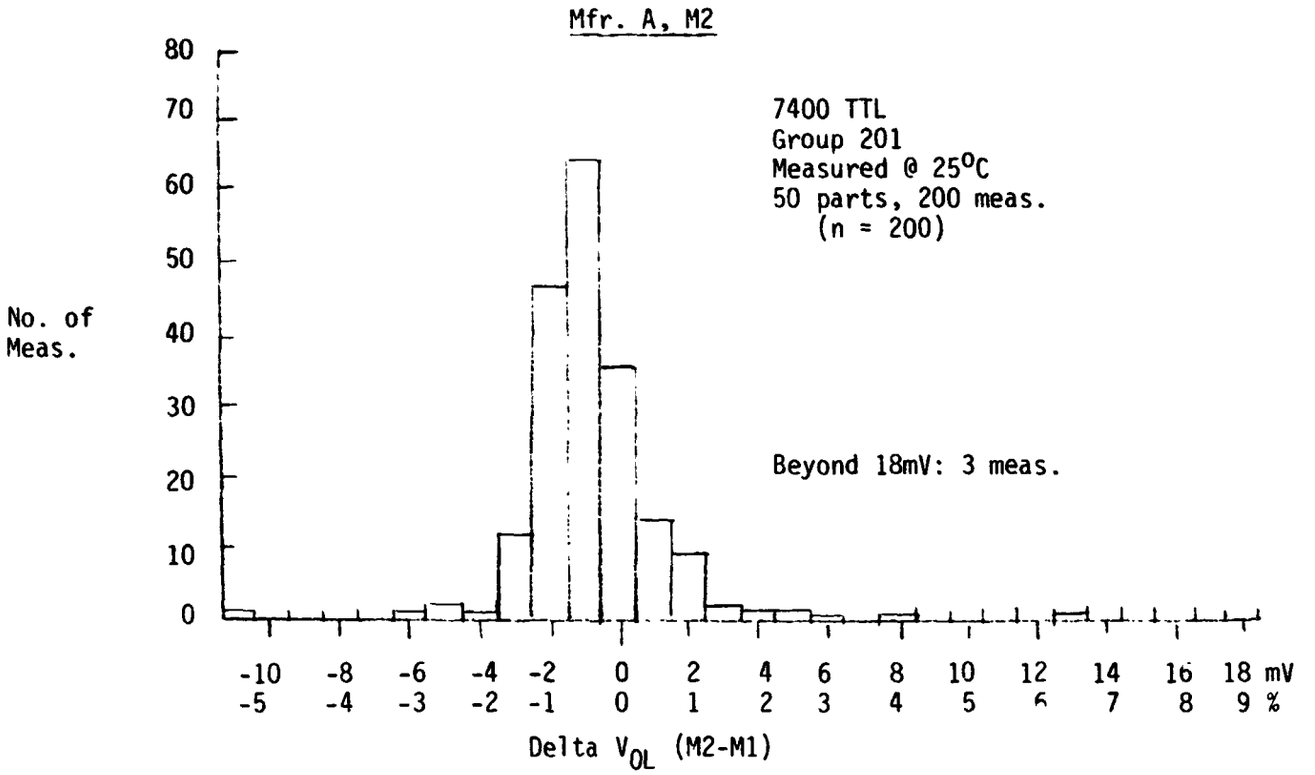


Figure B-35. Distribution of Delta V_{OL} After Thermal Shock

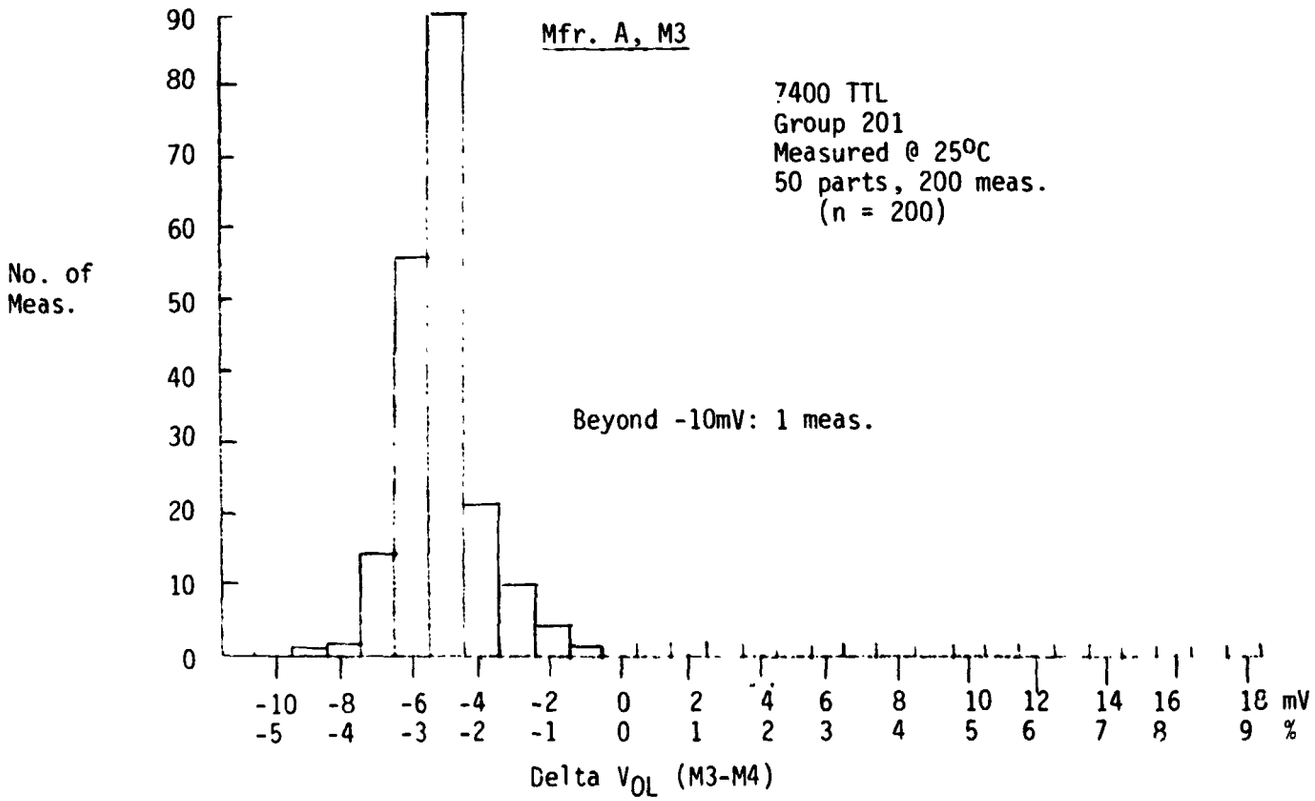


Figure B-36. Distribution of Delta V_{OL} After Moisture Resistance

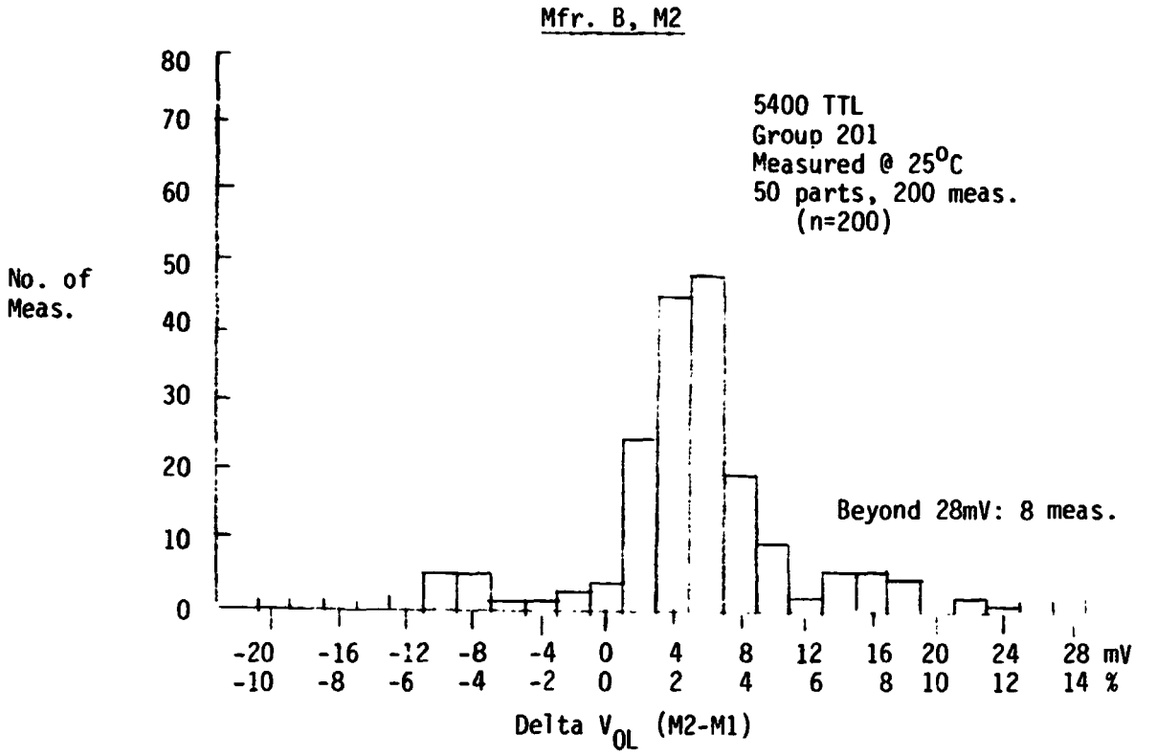


Figure B-37. Distribution of Delta V_{OL} After Thermal Shock

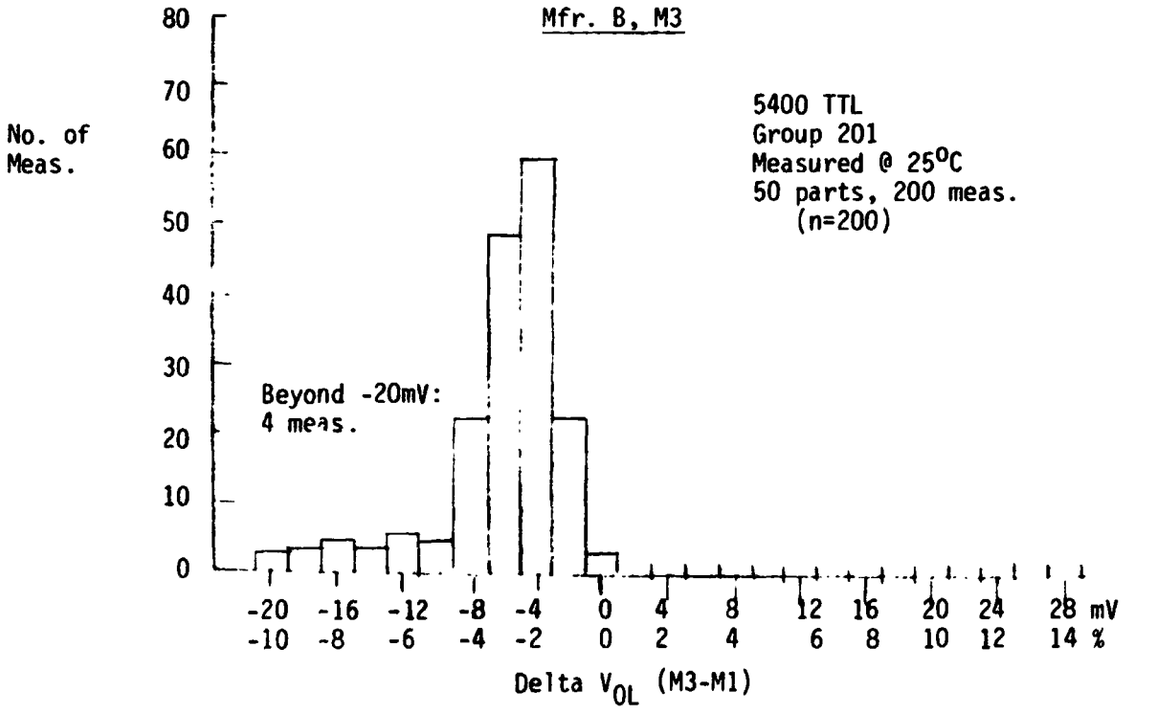


Figure B-38. Distribution of Delta V_{OL} After Moisture Resistance

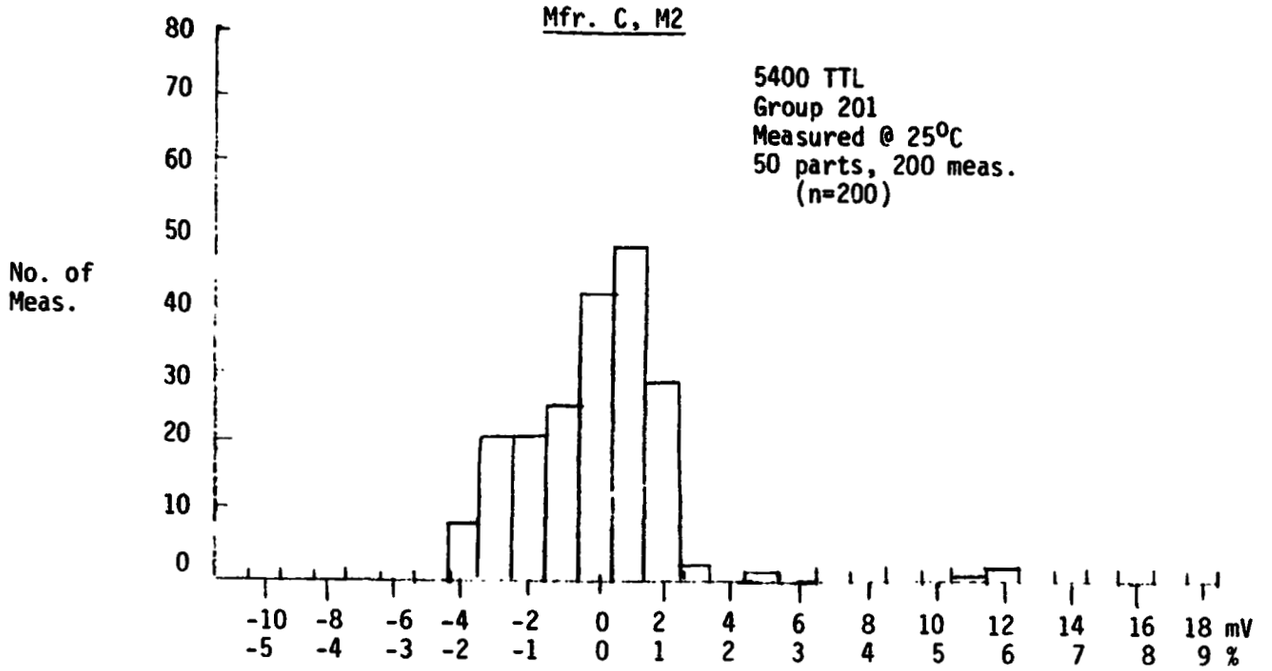


Figure B-39. Distribution of Delta V_{OL} After Thermal Shock

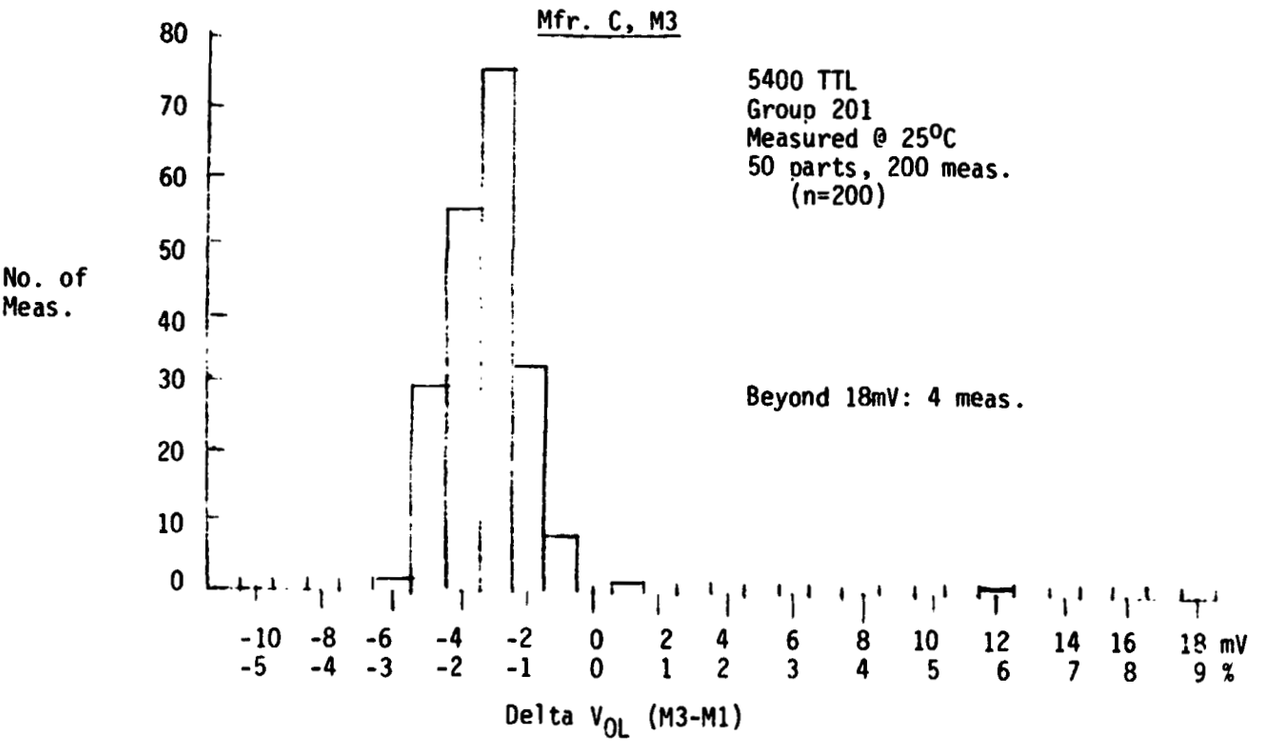


Figure B-40. Distribution of Delta V_{OL} After Moisture Resistance

Series d

The following sequence of histograms shows the variations in V_{OH4} and V_{OL2} for Manufacturer E 4007 CMOS Group 201 parts measured at 125°C for M1, M2, M3, M4, and M5.

Since there are three outputs for each part, a total of 150 measurements are possible in a 50 part group. These measurements are all combined in each histogram. See Table 3-4c for definition of the V_{OH4} and V_{OL2} measurement forcing functions.

The data is presented with the V_{OH4} and V_{OH2} histograms both on one page, with succeeding measurement increments (M1, M2, etc.) on succeeding pages.

Table B-5. Series d Histograms

Part Type	Mfr.	Measurement	201	202	203	204	205	206	207
7400 TTL	A	M1							
		M2							
		M3							
		M4							
		M5							
5400 TTL	B	M1							
		M2							
		M3							
		M4							
		M5							
5400 TTL	C	M1							
		M2							
		M3							
		M4							
		M5							
7400 TTL	D	M1							
		M2							
		M3							
		M4							
		M5							
4007 CMOS	E	M1	d						
		M2	d						
		M3	d						
		M4	d						
		M5	d						
4007 CMOS	C	M1							
		M2							
		M3							
		M4							
		M5							
741 Linear	E	M1							
		M2							
		M3							
		M4							
		M5							

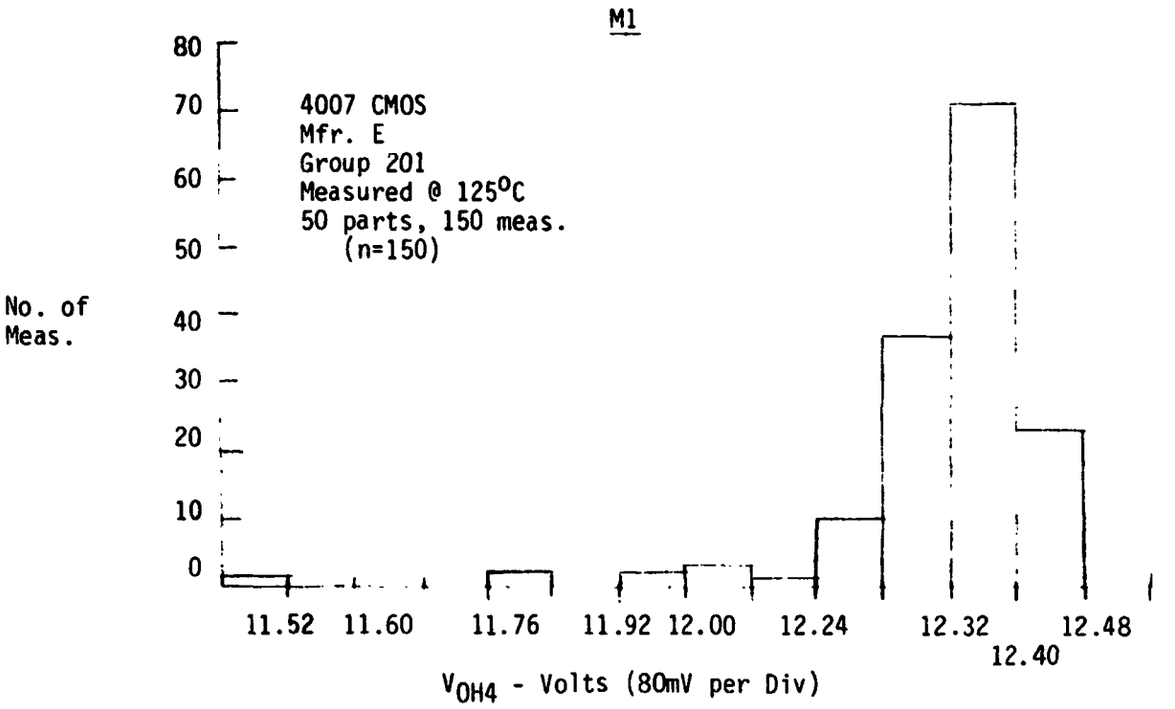


Figure B-41. Initial Distribution of V_{OH4}

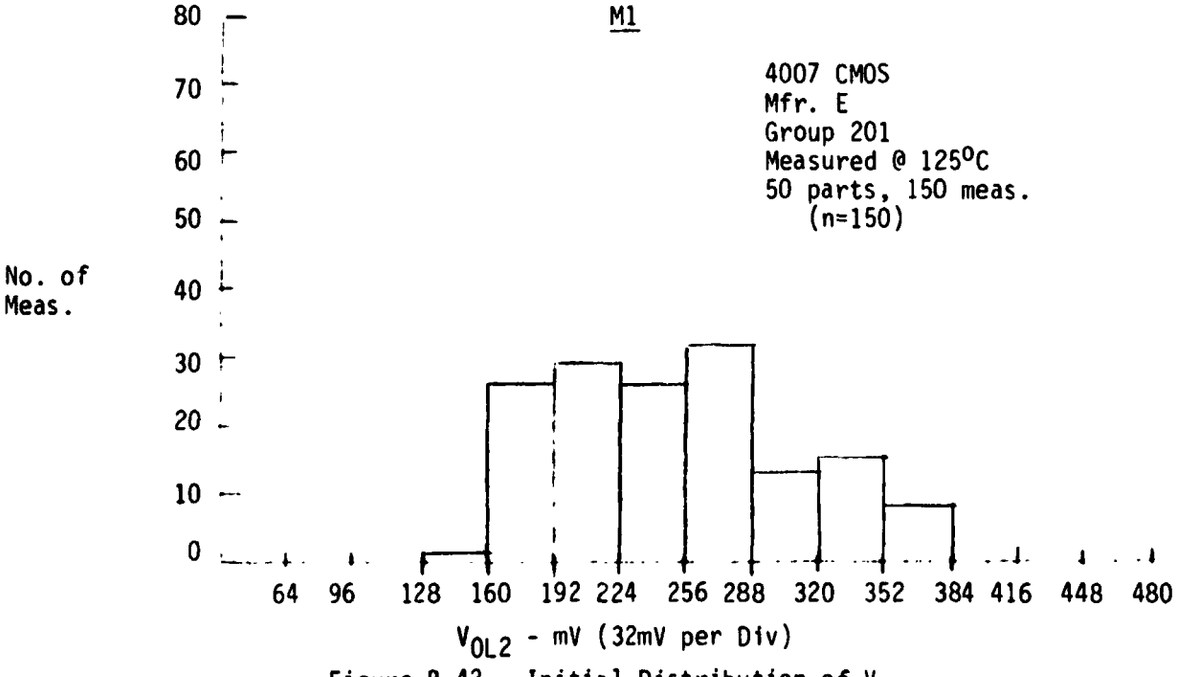


Figure B-42. Initial Distribution of V_{OL2}

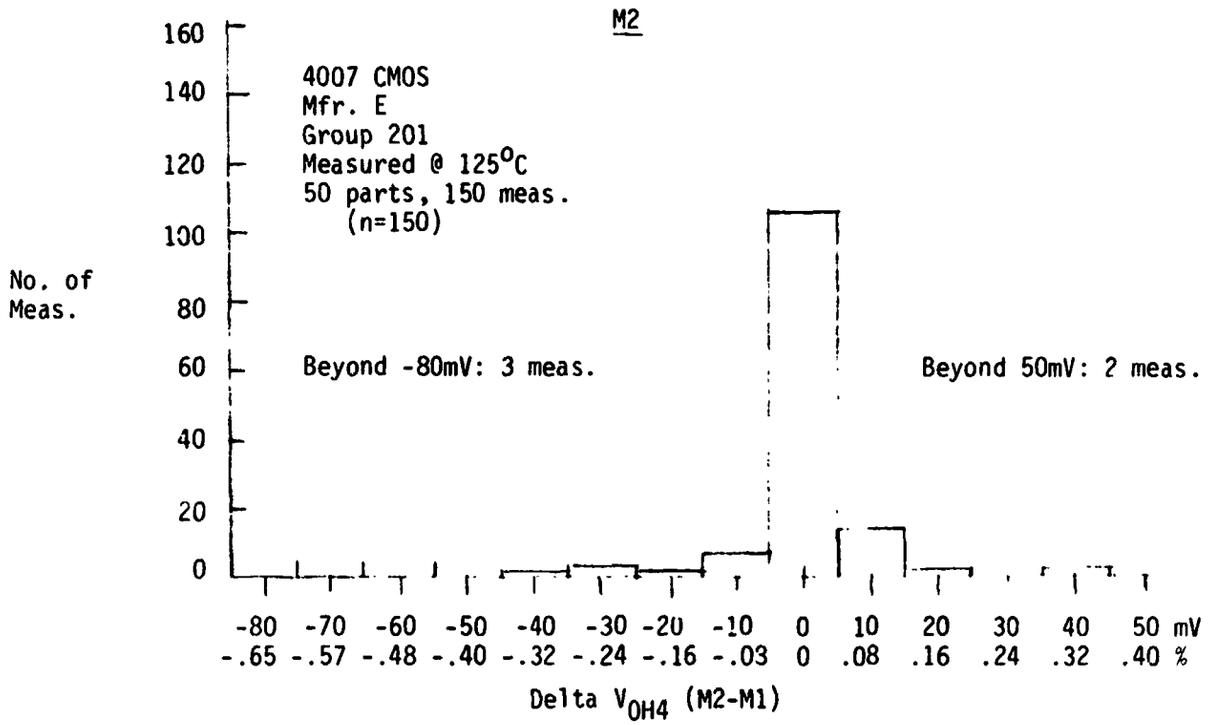


Figure B-43. Distribution of Delta V_{OH4} After Thermal Shock

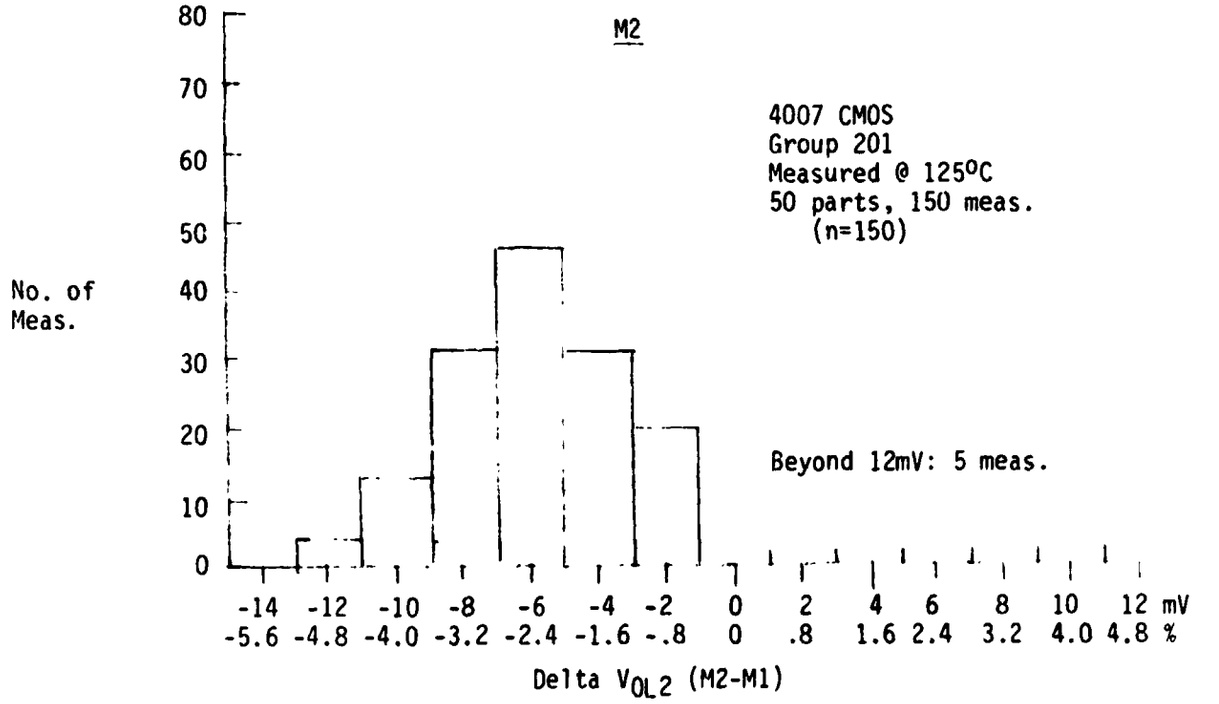


Figure B-44. Distribution of Delta V_{OL2} After Thermal Shock

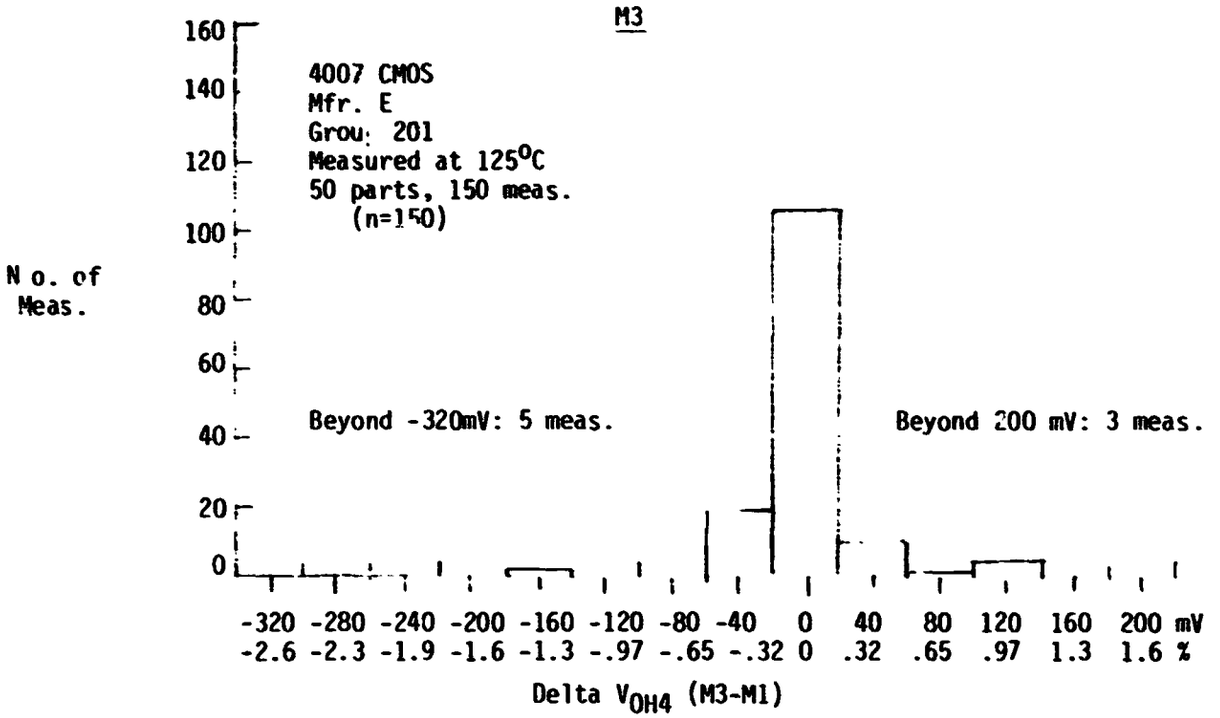


Figure B-5. Distribution of lelta V_{OH4} After Moisture Resistance

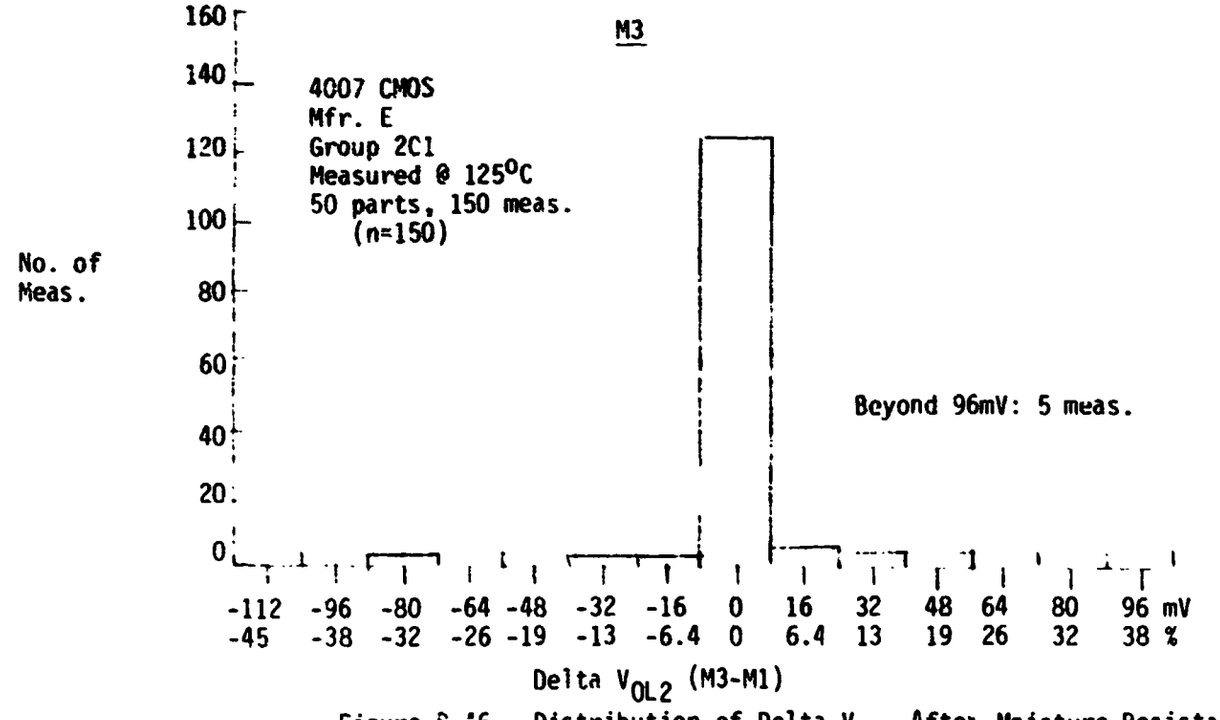


Figure B-46. Distribution of Delta V_{OL2} After Moisture Resistance

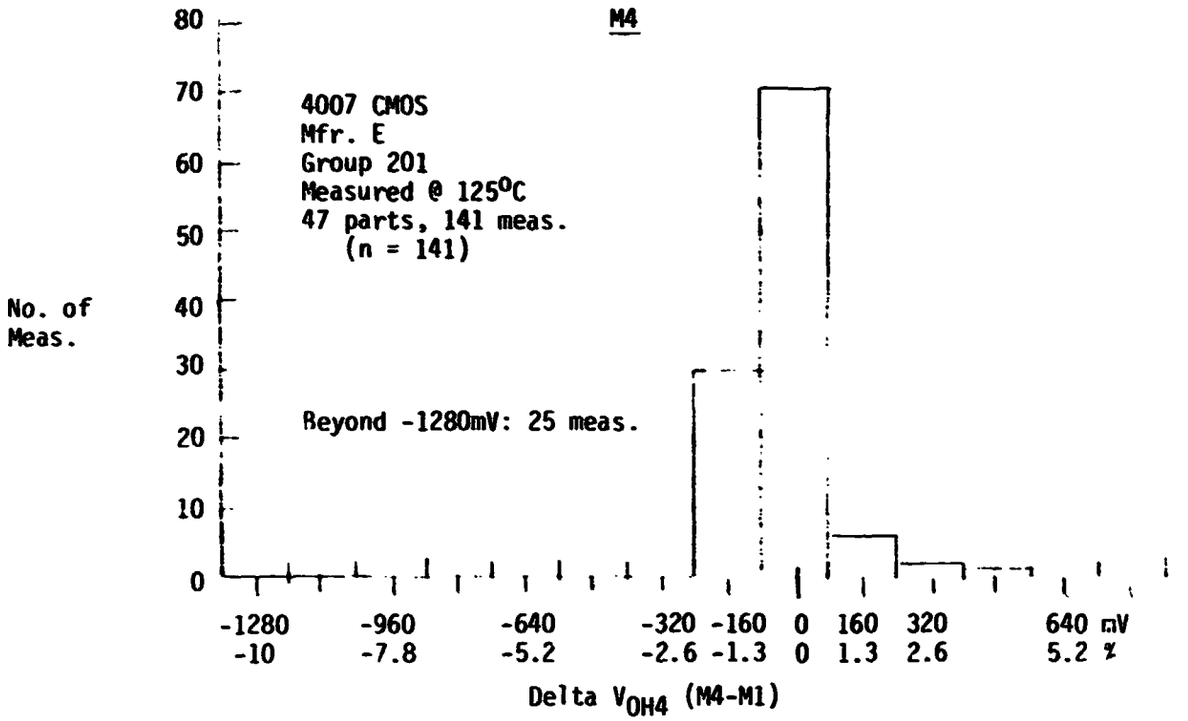


Figure B-47. Distribution of Delta V_{OH4} After Low Temp Life

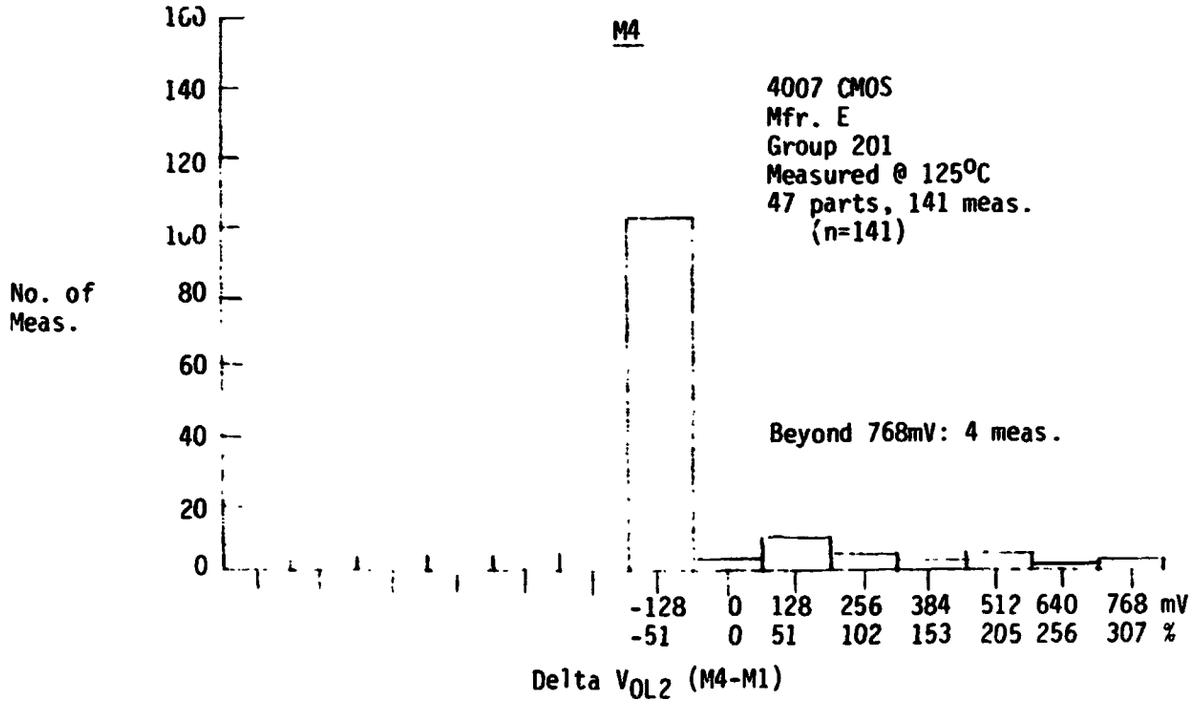


Figure B-48. Distribution of Delta V_{OL2} After Low Temp Life

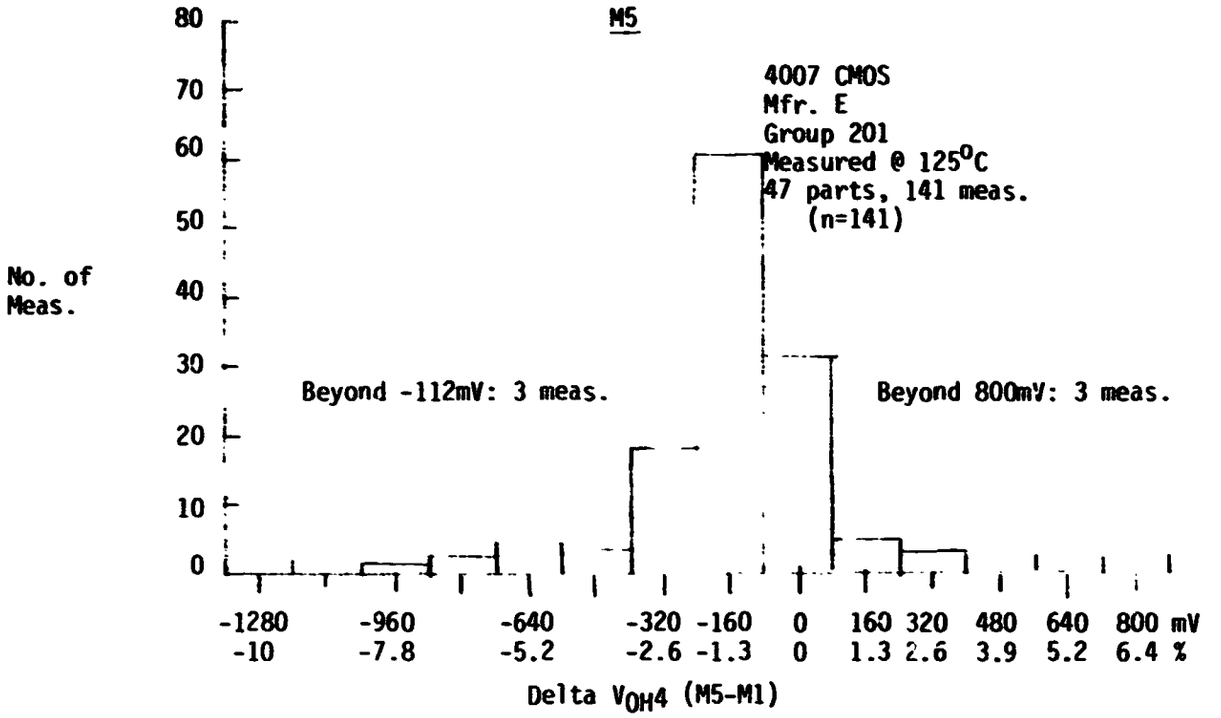


Figure B-49. Distribution of Delta V_{OH4} After Hi Temp Life

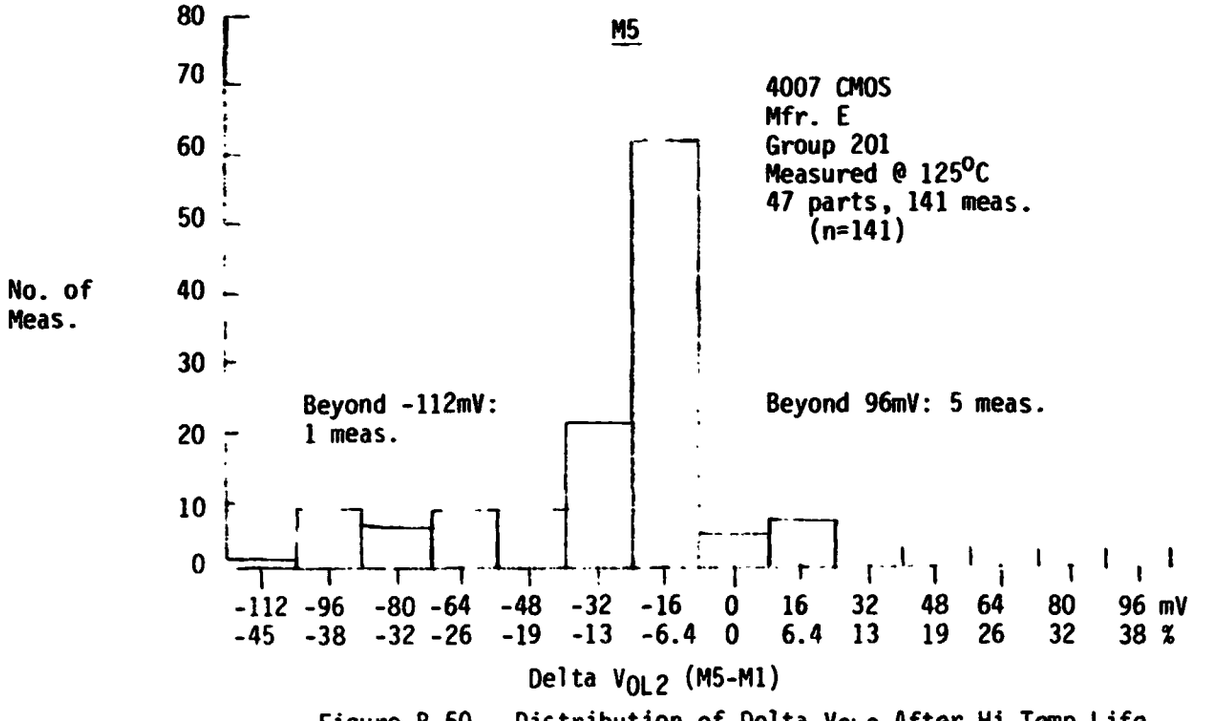


Figure B-50. Distribution of Delta V_{OL2} After Hi Temp Life

Series e

The following sequence of histograms shows the variation in V_{OH4} and V_{OL2} measured at 125°C at M4 for Manufacturer E parts in each of the environmental stress groups 202 through 207. All three V_{OH4} or V_{OL2} measurements on each part are combined in the histograms. For the corresponding Group 201 distribution, see Figures B-47 and B-48. For a complete definition of the prior environments experienced by each group, refer to Figure 3-4.

Table B-6. Series e Histograms

Part Type	Mfr.	Measurement	201	202	203	204	205	206	207
7400 TTL	A	M1							
		M2							
		M3							
		M4							
		M5							
5400 TTL	B	M1							
		M2							
		M3							
		M4							
		M5							
5400 TTL	C	M1							
		M2							
		M3							
		M4							
		M5							
7400 TTL	D	M1							
		M2							
		M3							
		M4							
		M5							
4007 CMOS	E	M1							
		M2							
		M3							
		M4	e*	e	e	e	e	e	e
		M5							
4007 CMOS	C	M1							
		M2							
		M3							
		M4							
		M5							
741 Linear	E	M1							
		M2							
		M3							
		M4							
		M5							

* Figures B-47, B-48.

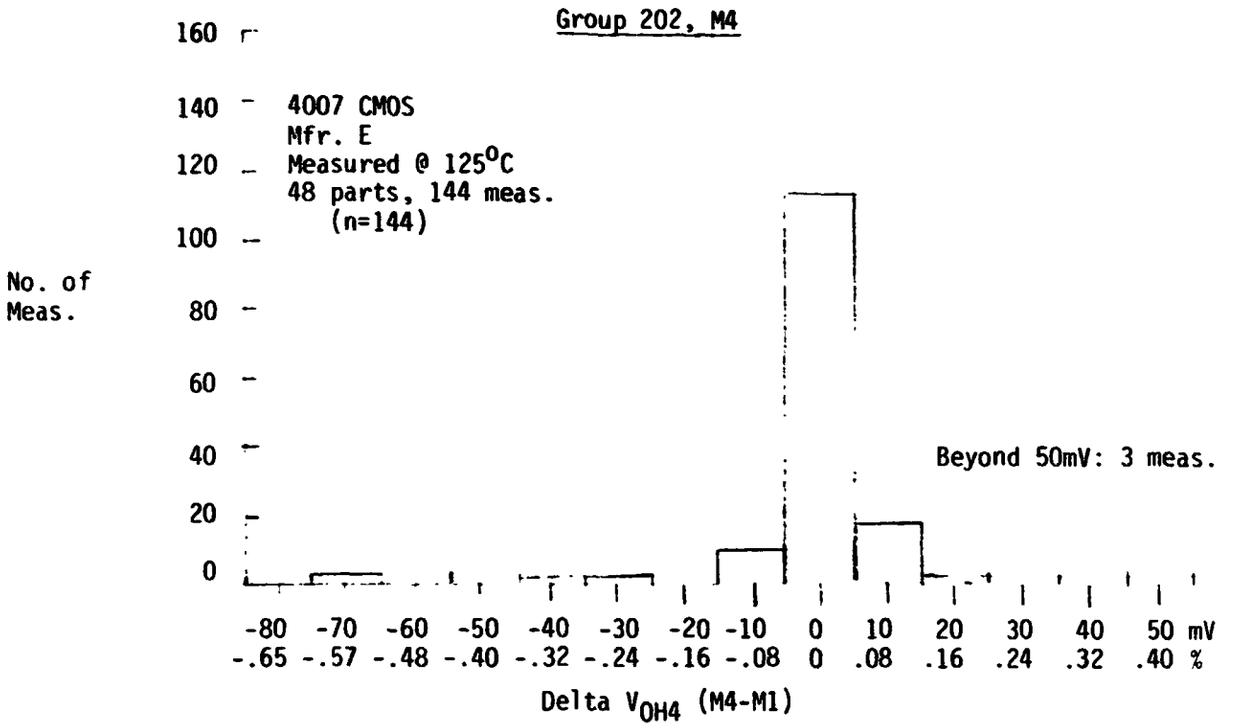


Figure B-51. Distribution of Delta V_{OH4} After 4000 Temp Cycles

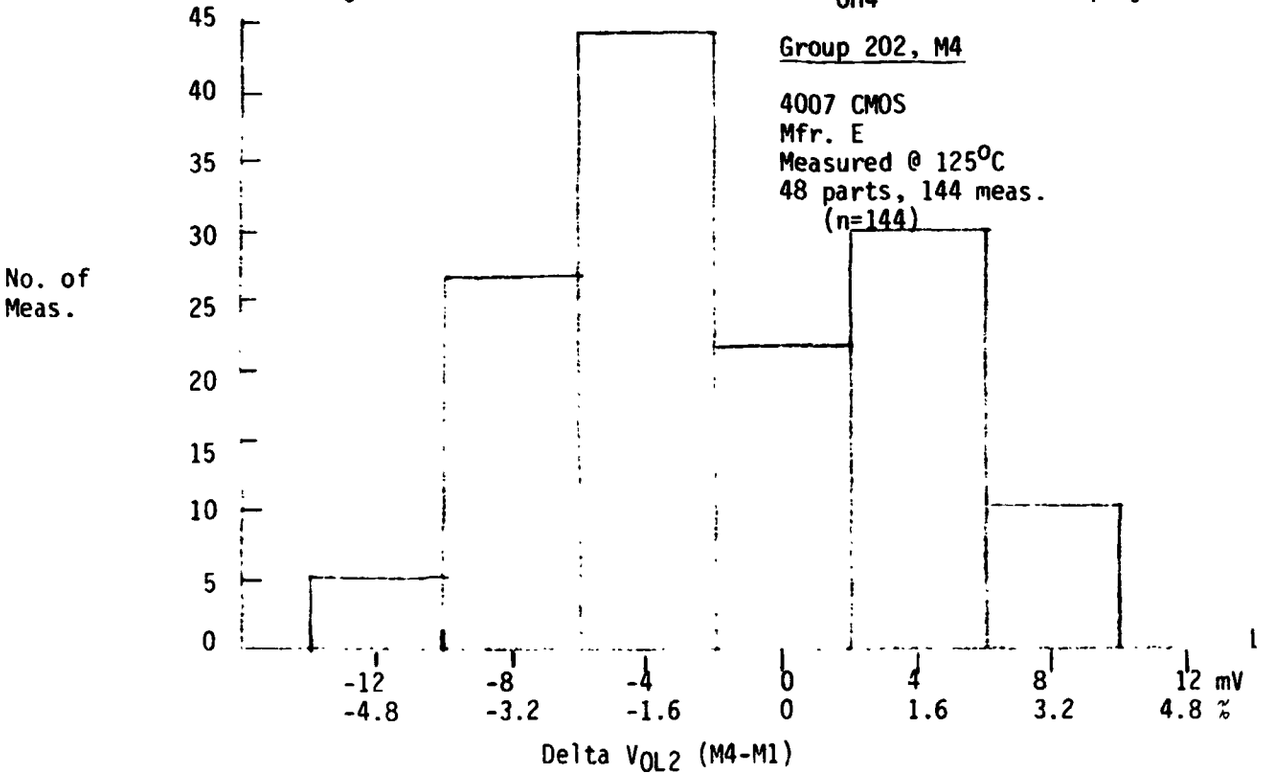


Figure B-52. Distribution of Delta V_{OL2} After 4000 Temp Cycles

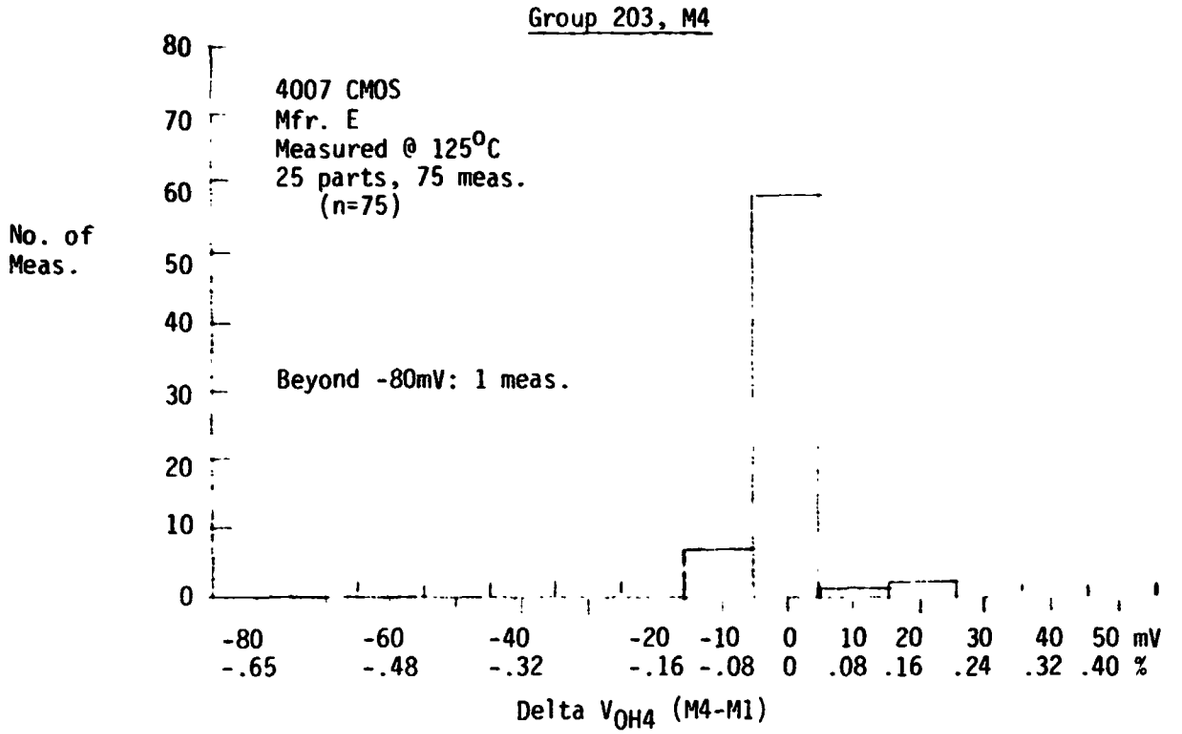


Figure B-53. Distribution of Delta V_{OH4} After 70g Vibration

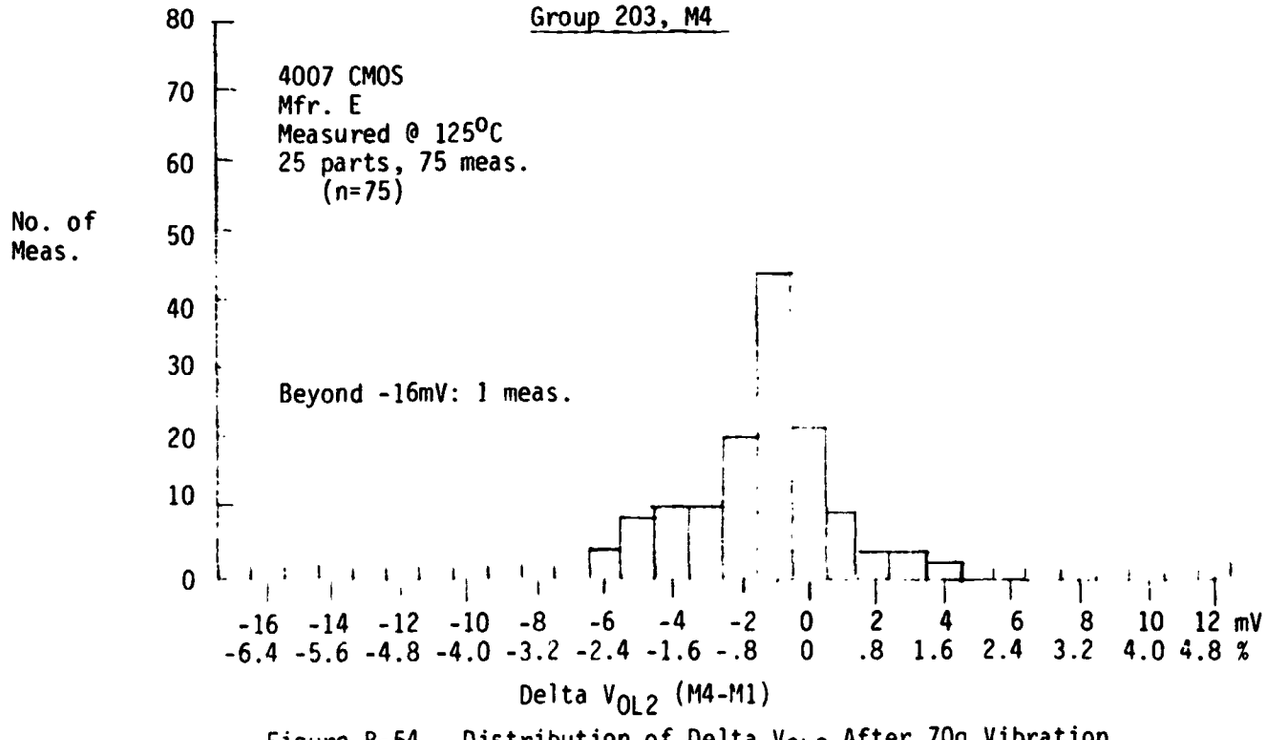


Figure B-54. Distribution of Delta V_{OL2} After 70g Vibration

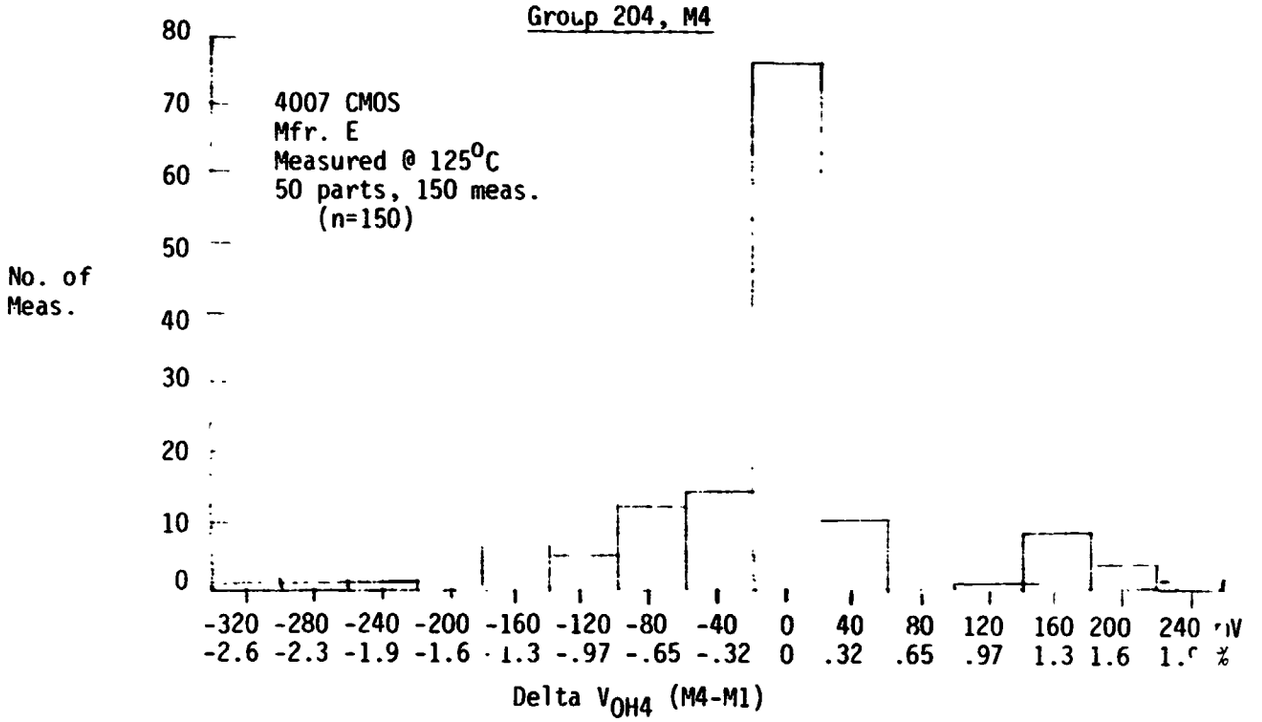


Figure B-55. Distribution of Delta V_{OH4} After Vacuum Life

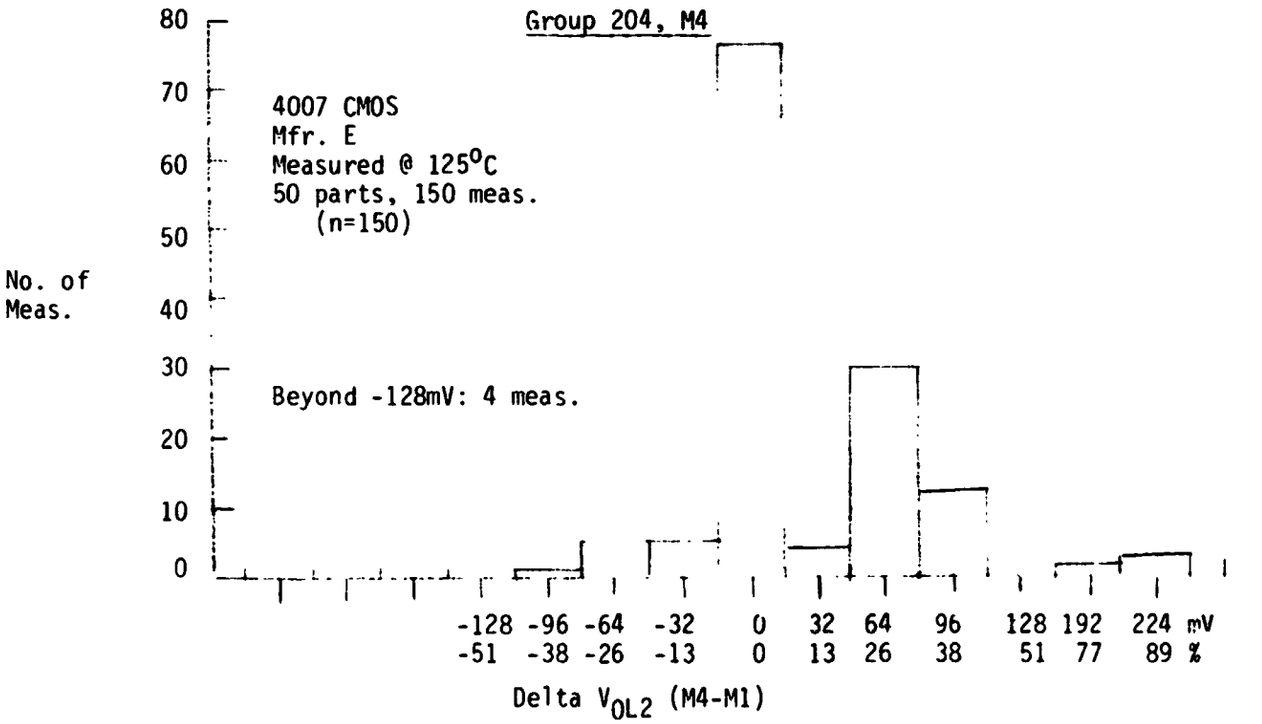


Figure B-56. Distribution of Delta V_{OL2} After Vacuum Life

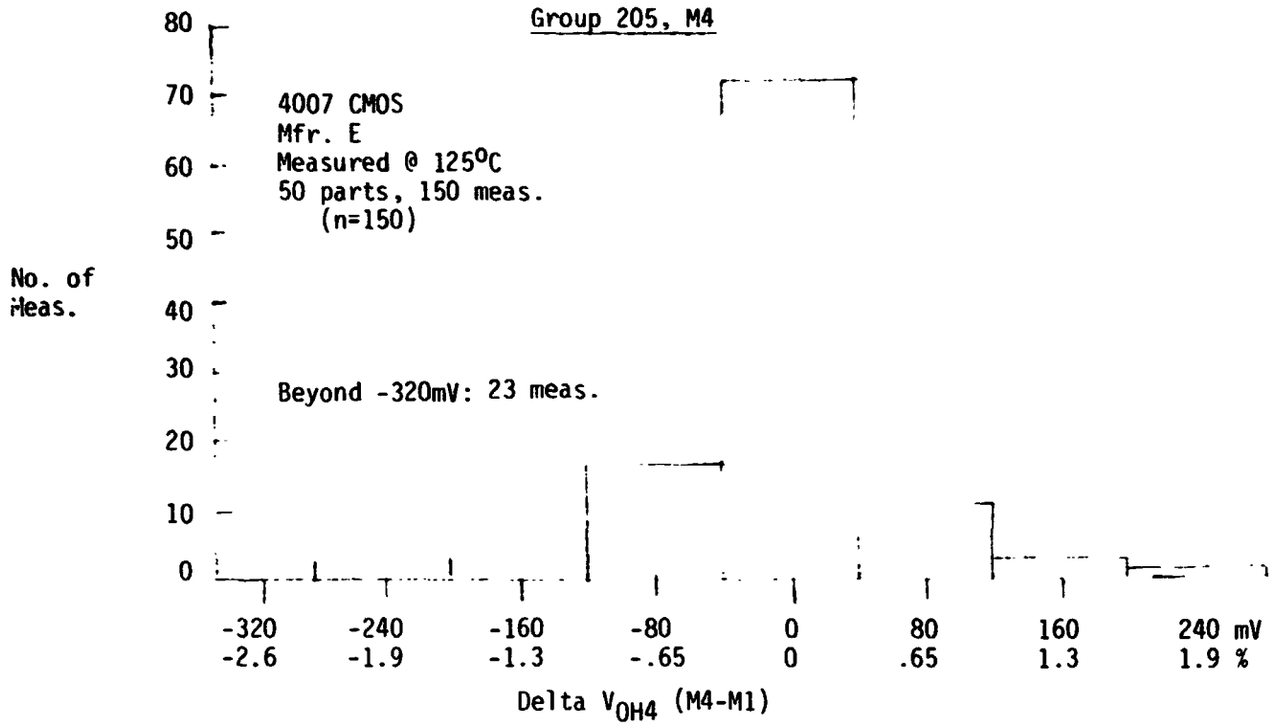


Figure B-57. Distribution of Delta V_{OH4} After Low Temp Life

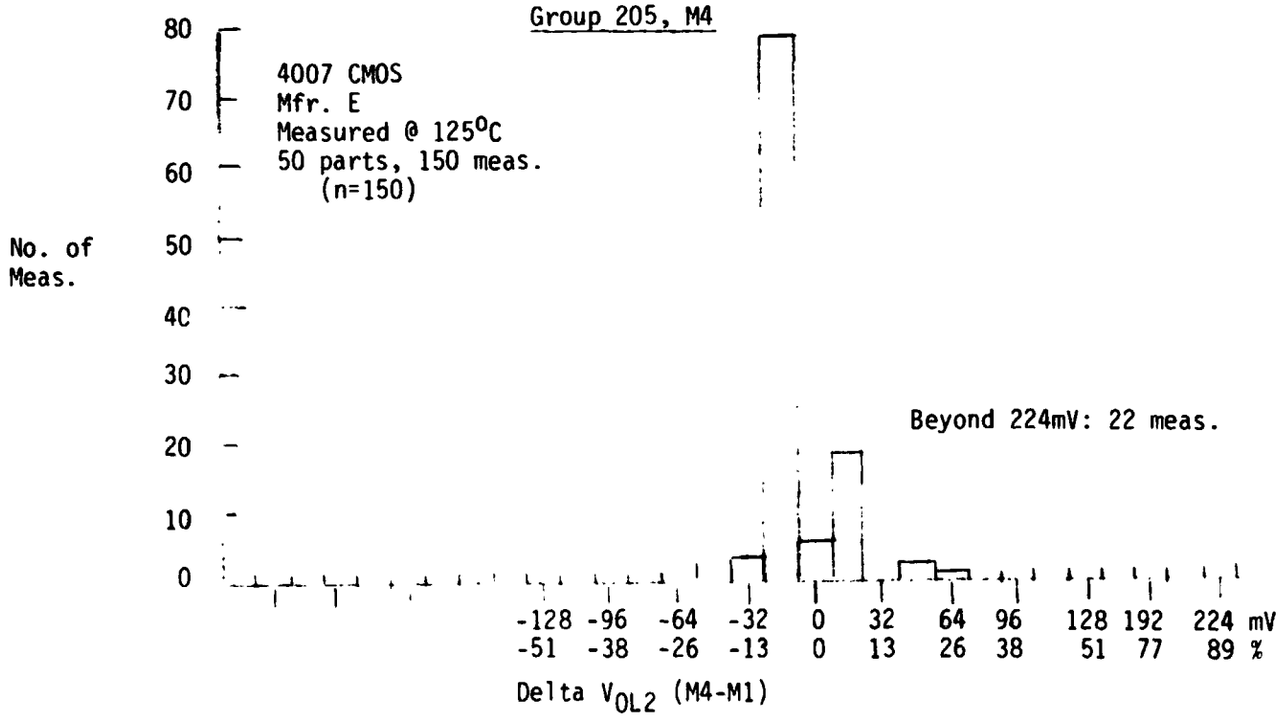


Figure B-58. Distribution of Delta V_{OL2} After Low Temp Life

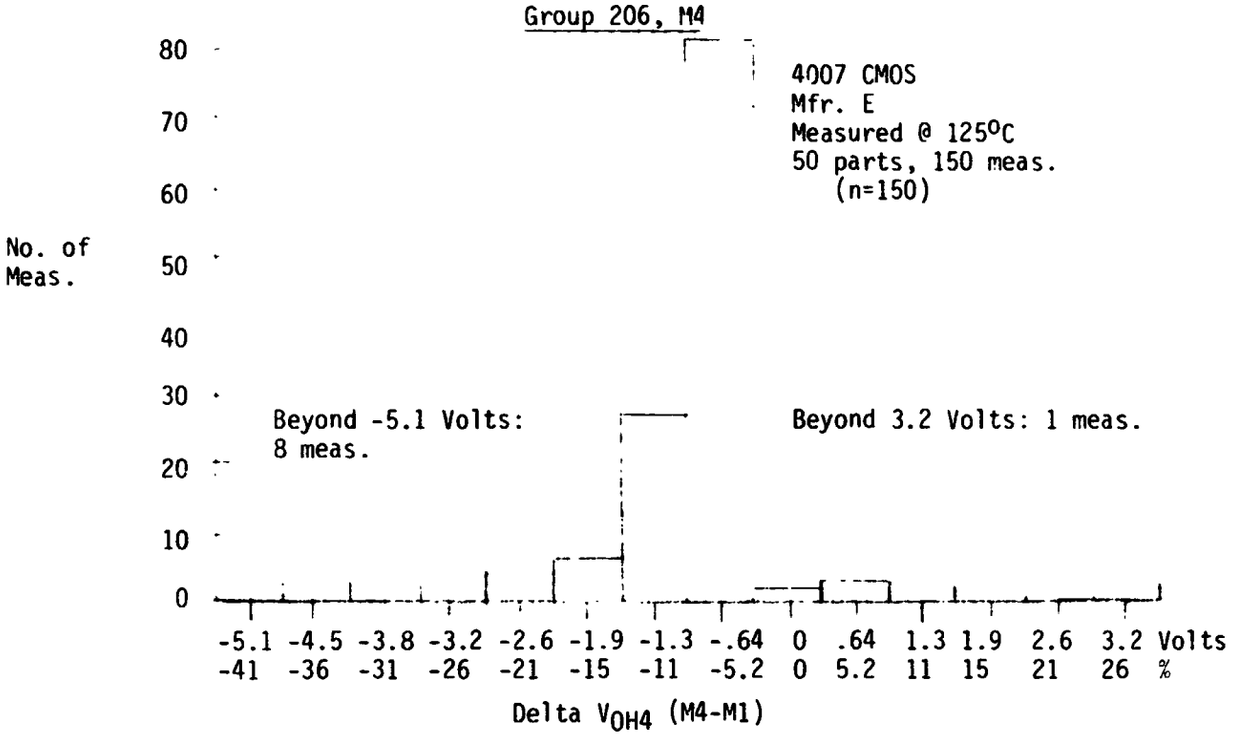


Figure B-59. Distribution of Delta V_{OH4} After Hi Temp Life

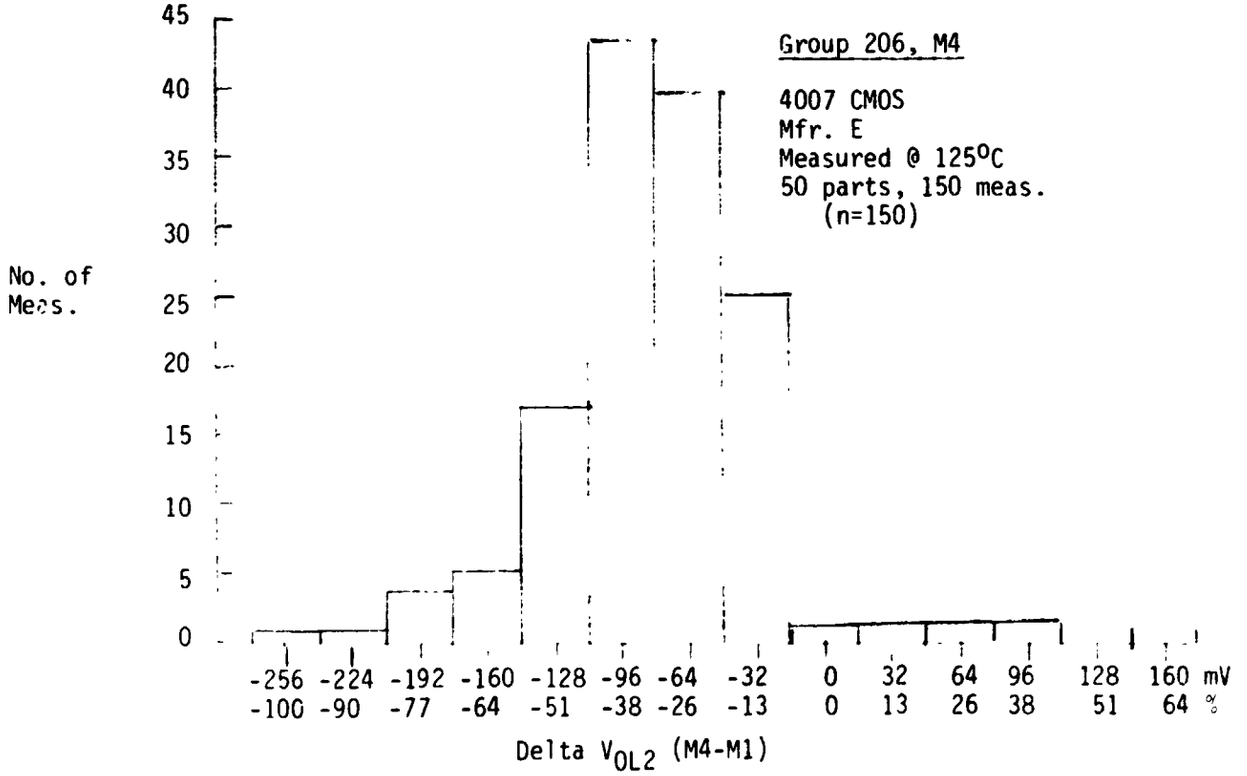


Figure B-60. Distribution of Delta V_{OL2} After Hi Temp Life

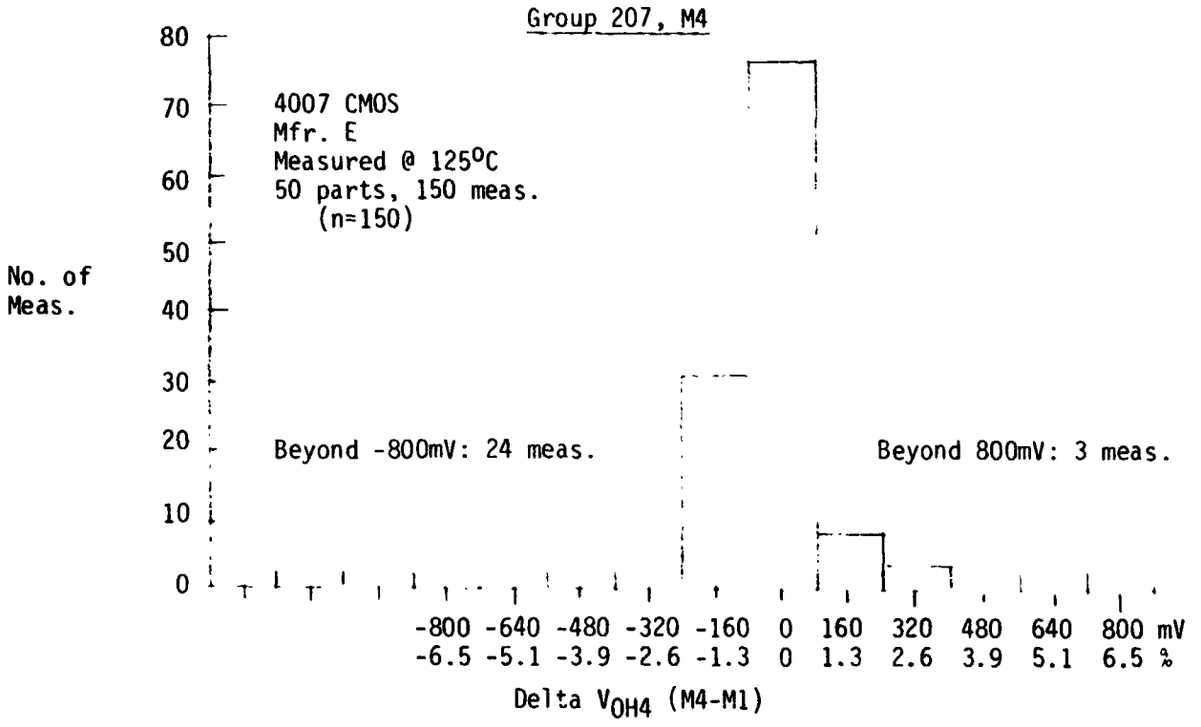


Figure B-61. Distribution of Delta V_{OH4} After Low Temp Life

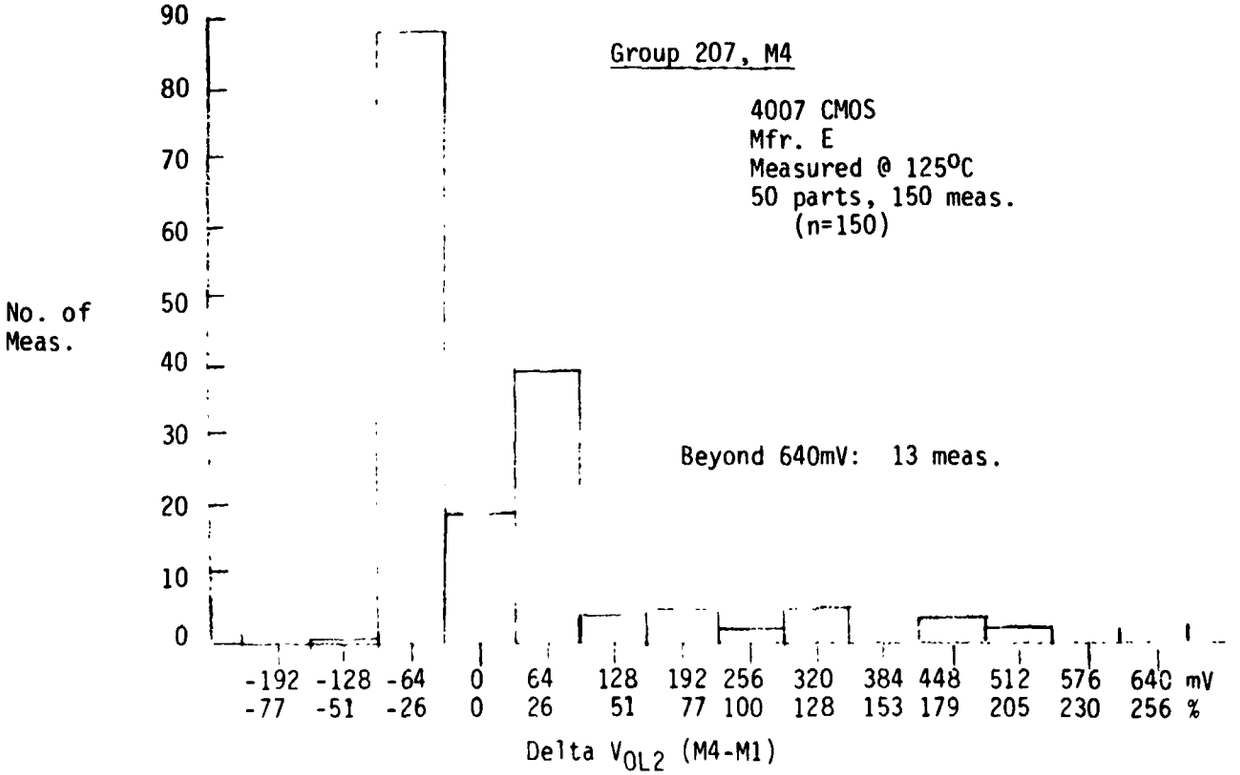


Figure B-62. Distribution of Delta V_{OL2} After Low Temp Life

REPORT DOCUMENTATION PAGE

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18. SUPPLEMENTARY NOTES

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19 KEY WORDS (Continue on reverse side if necessary and identify by block number)

Plastic Microcircuits	Screening	Channeling
Encapsulated Microcircuits	Qualificat on	TTL Microcircuits
Novolac Epoxy Microcircuits	Environmental Testing	CMOS Microcircuits
Stress Testing	Failure Mechanisms	Linear Microcircuits
Space Applications	Plague	Gold Metallization

20 ABSTRACT (Continue on reverse side if necessary and identify by block number)

Environmental stress tests were performed on novolac epoxy encapsulated microcircuits to determine their capability of performing in space applications and environments. Various Thermal, vibration, thermal cycling, and reduced barometric pressure stress tests were performed to obtain electrical, environmental and failure data. Analyses of data obtained were employed to derive information on environmental and operating design limits, effects of single and multiple levels and effects of stress levels on failure rates. Seven different

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19. (Continued)

Thermal Cycling	HTOT	Plastic Plague
Humidity Cycling	Ruptures Plastic	Stress Corrosion Cracking
Vacuum Life Test	Broken Bond Wires	Accelerated Testing
Operating Life Test	Peripheral Opens	

20. (Continued)

part types (four TTL, two CMOS, one linear) from five different manufacturers were tested.

The results showed that solid encapsulated TTL (bipolar) microcircuits are very stable and performed very well; linear bipolar microcircuits suffered from thermal runaway; CMOS microcircuits are so unstable that no further study should be performed on them. For TTL microcircuits, a recommended qualification test is a high temperature operating life test at 175°C, and a recommended screening test is three-temperature (-55°C, 25°C, +125°C) electrical measurement in lieu of any other screens.